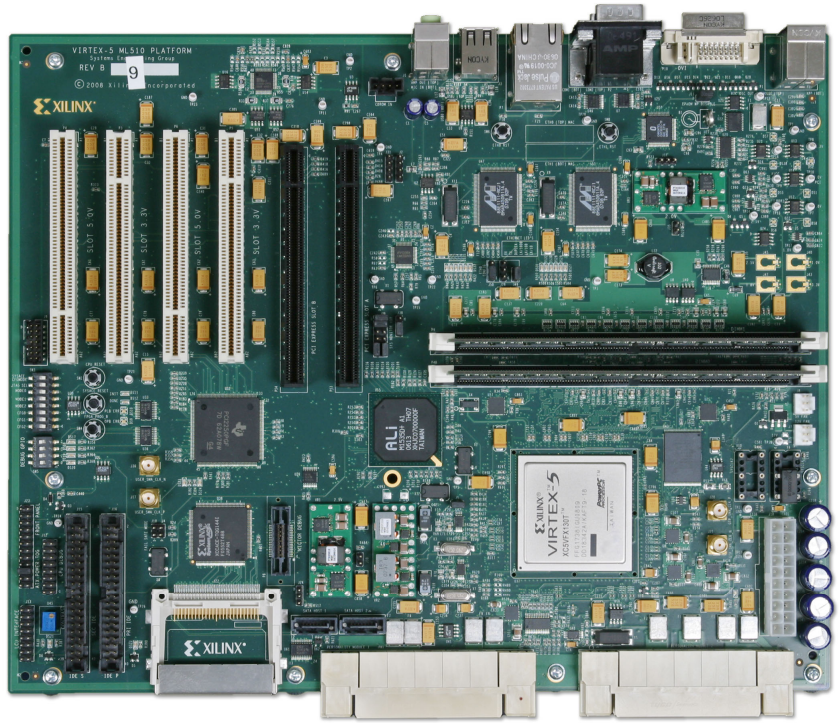
ML510 QuickStart



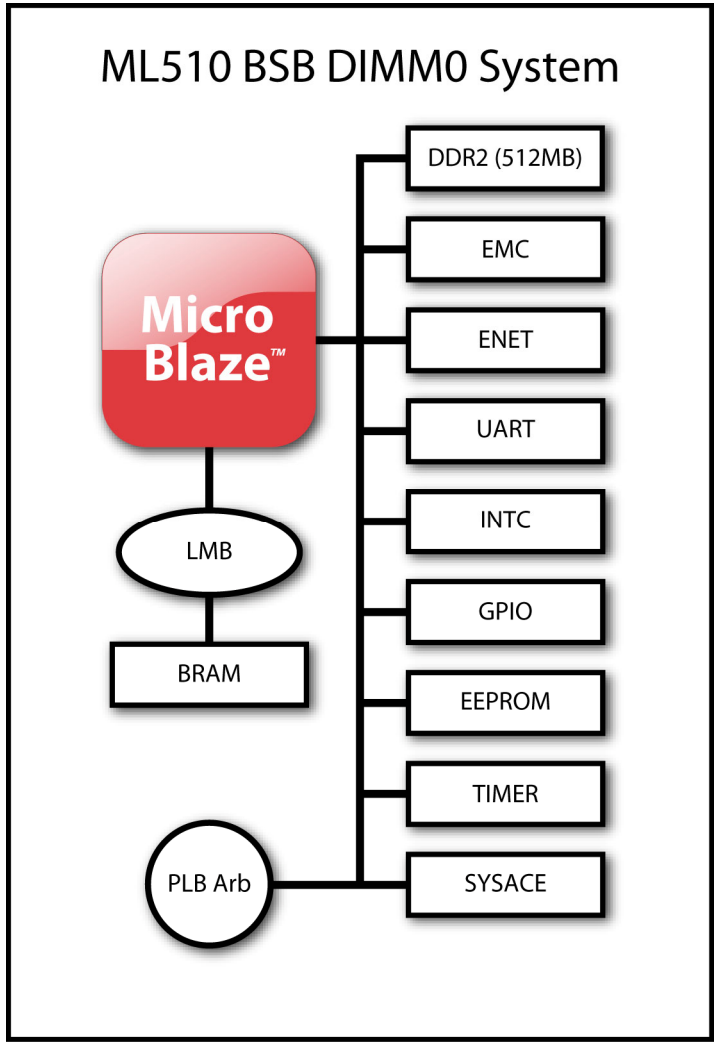
August 2008

Overview

- Setup
- Boot with ACE-loader ACE File
- Observe LCD and Terminal messages
- Load new Configuration
- Re-load ACE-loader

ML510 BSB DIMM0 Hardware

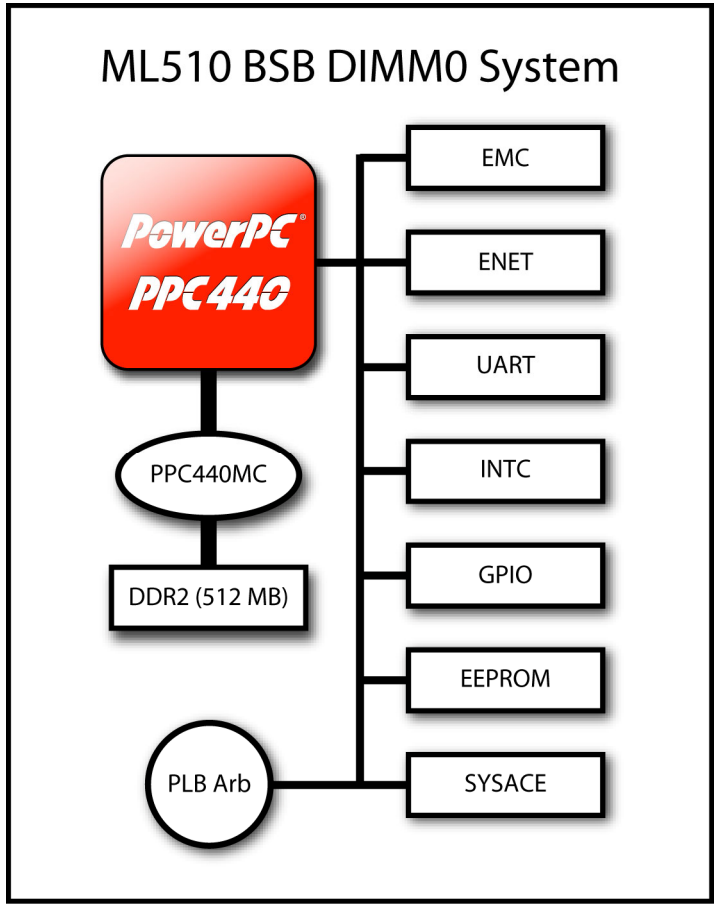
- The ML510 MicroBlaze design hardware includes:
  - DDR2 Interface (512 MB)
  - BRAM
  - External Memory Controller (EMC)
  - Networking
  - UART
  - Interrupt Controller
  - GPIO
  - EEPROM (IIC and SPI)
  - Timer
  - System ACE CF Interface
  - PLB Arbiter



Note: Presentation applies to the ML510

ML510 BSB DIMM0 Hardware

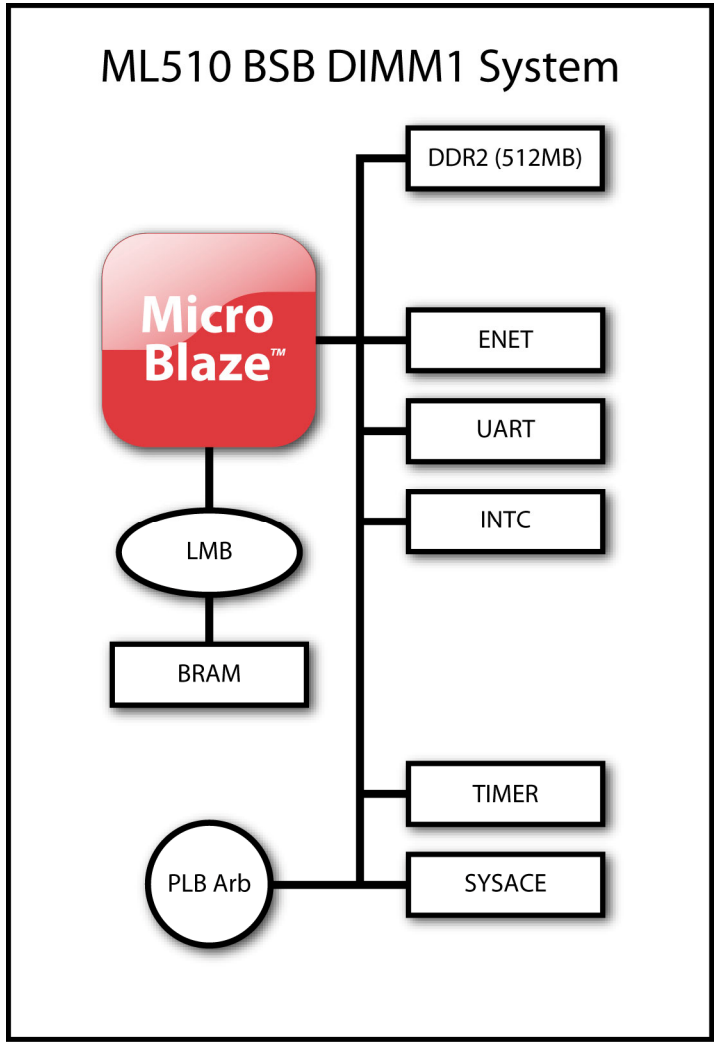
- The ML510 PPC440 design hardware includes:
  - DDR2 Interface (512 MB)
  - BRAM
  - External Memory Controller (EMC)
  - Networking
  - UART
  - Interrupt Controller
  - GPIO
  - EEPROM (IIC and SPI)
  - Timer
  - System ACE CF Interface
  - PLB Arbiter



Note: Presentation applies to the ML510

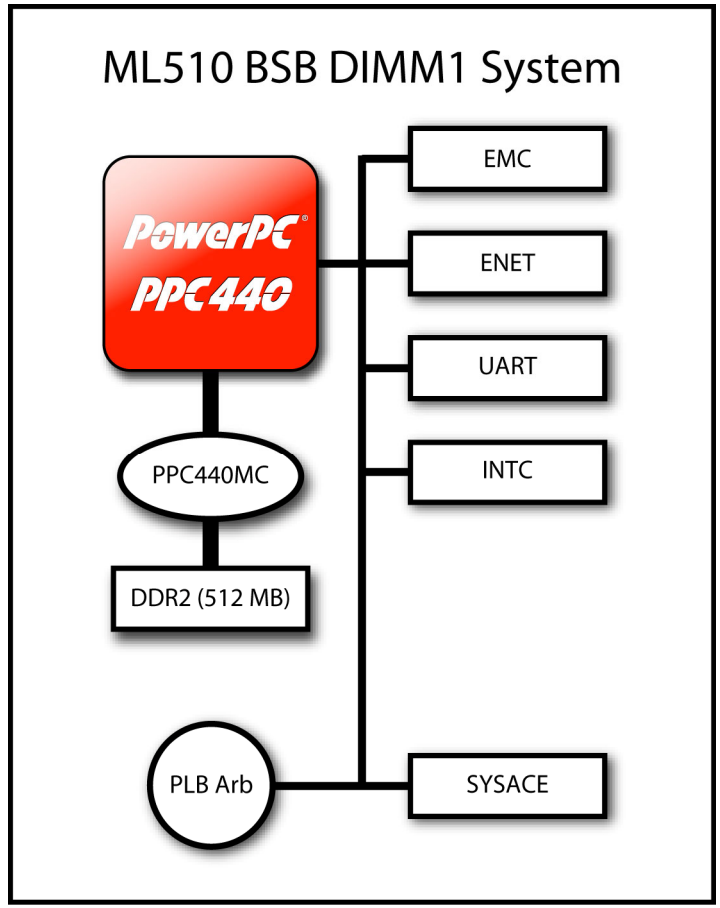
ML510 BSB DIMM1 Hardware

- The ML510 MicroBlaze design hardware includes:
  - DDR2 Interface (512 MB)
  - BRAM
  - Networking
  - UART
  - Interrupt Controller
  - Timer
  - System ACE CF Interface
  - PLB Arbiter



ML510 BSB DIMM1 Hardware

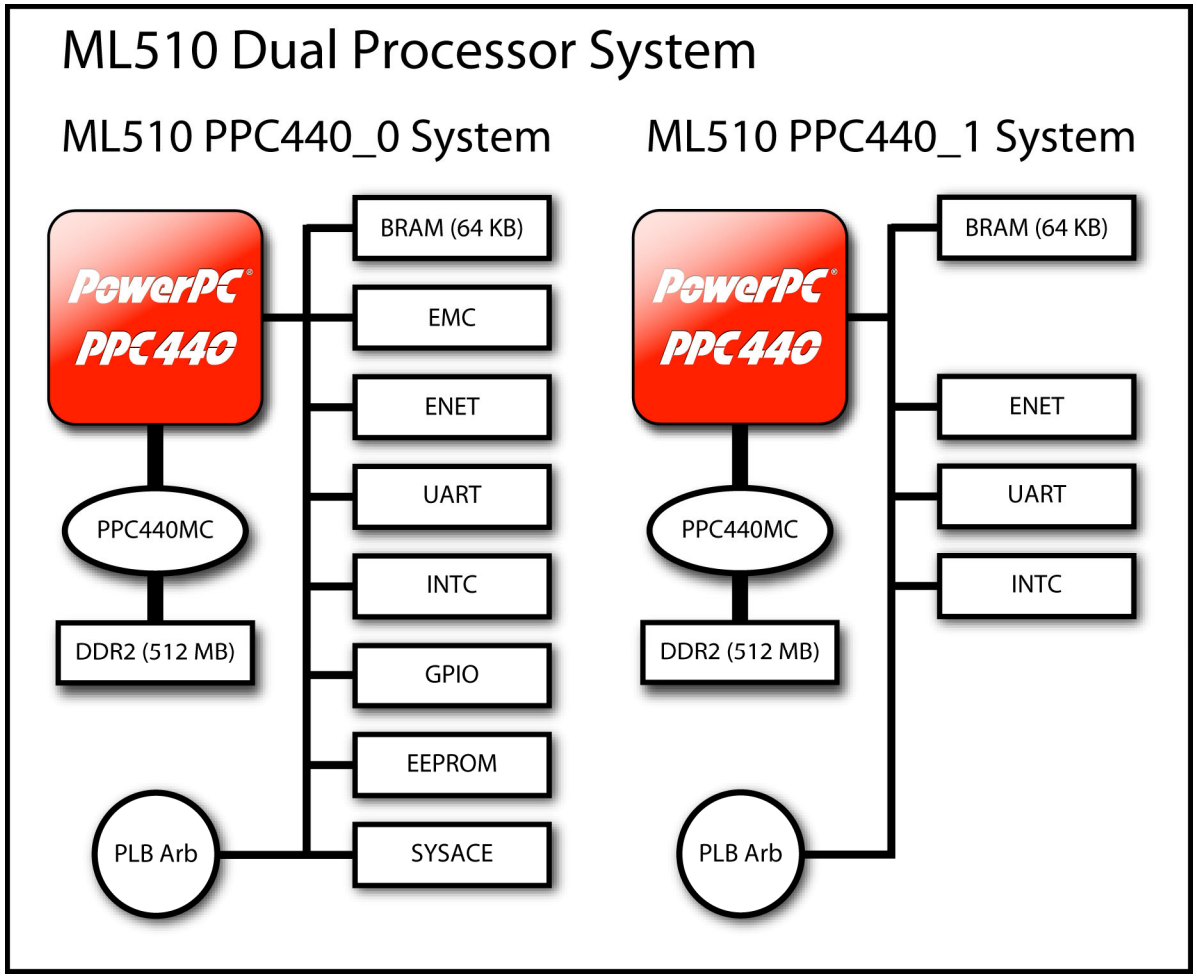
- The ML510 PPC440 design hardware includes:
  - DDR2 Interface (512 MB)
  - BRAM
  - External Memory Controller (EMC)
  - Networking
  - UART
  - Interrupt Controller
  - GPIO
  - EEPROM (IIC and SPI)
  - Timer
  - System ACE CF Interface
  - PLB Arbiter



Note: Presentation applies to the ML510

ML510 Dual Processor Hardware

- The ML510 Dual Processor design hardware includes:
- PPC440_0:
  - DDR2 Interface (512 MB)
  - BRAM (64 KB)
  - External Memory Controller
  - Networking
  - UART
  - Interrupt Controller
  - GPIO
  - EEPROM (IIC and SPI)
  - System ACE CF Interface
  - PLB Arbiter
- PPC440_1:
  - DDR2 Interface (512 MB)
  - BRAM (64 KB)
  - Networking
  - UART
  - Interrupt Controller
  - PLB Arbiter



Note: Presentation applies to the ML510

Additional Setup Details

- Refer to ml510_overview_setup.ppt for details on:
  - Software Requirements
  - ML510 Board Setup
    - **Equipment and Cables**
    - **Software**
    - **Network**
  - Terminal Programs
    - **This presentation requires the 9600-8-N-1 Baud terminal setup**

Note: Presentation applies to the ML510

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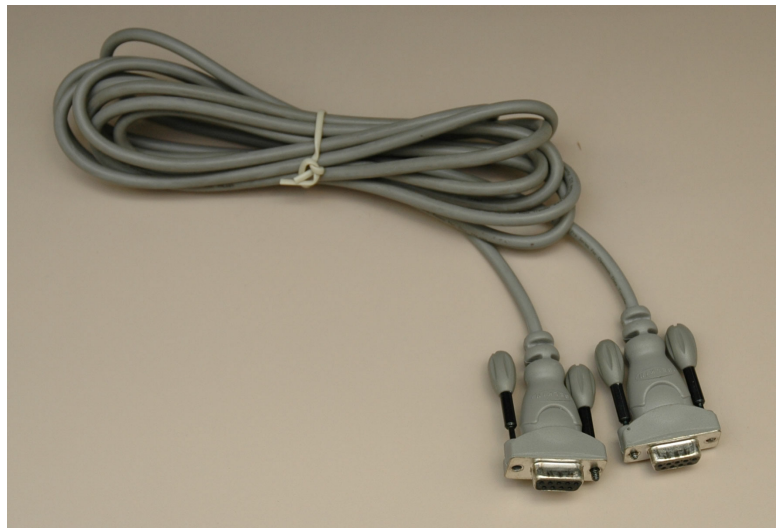
Hardware Setup

- Connect the Xilinx Parallel Cable IV (PC4) to the ML510 board

- Connect the RS232 null modem cable to the ML510 board



Note: Presentation applies to the ML510

Hardware Setup

- The ML510 uses a DVI video interface
- Connect a DVI monitor

  or

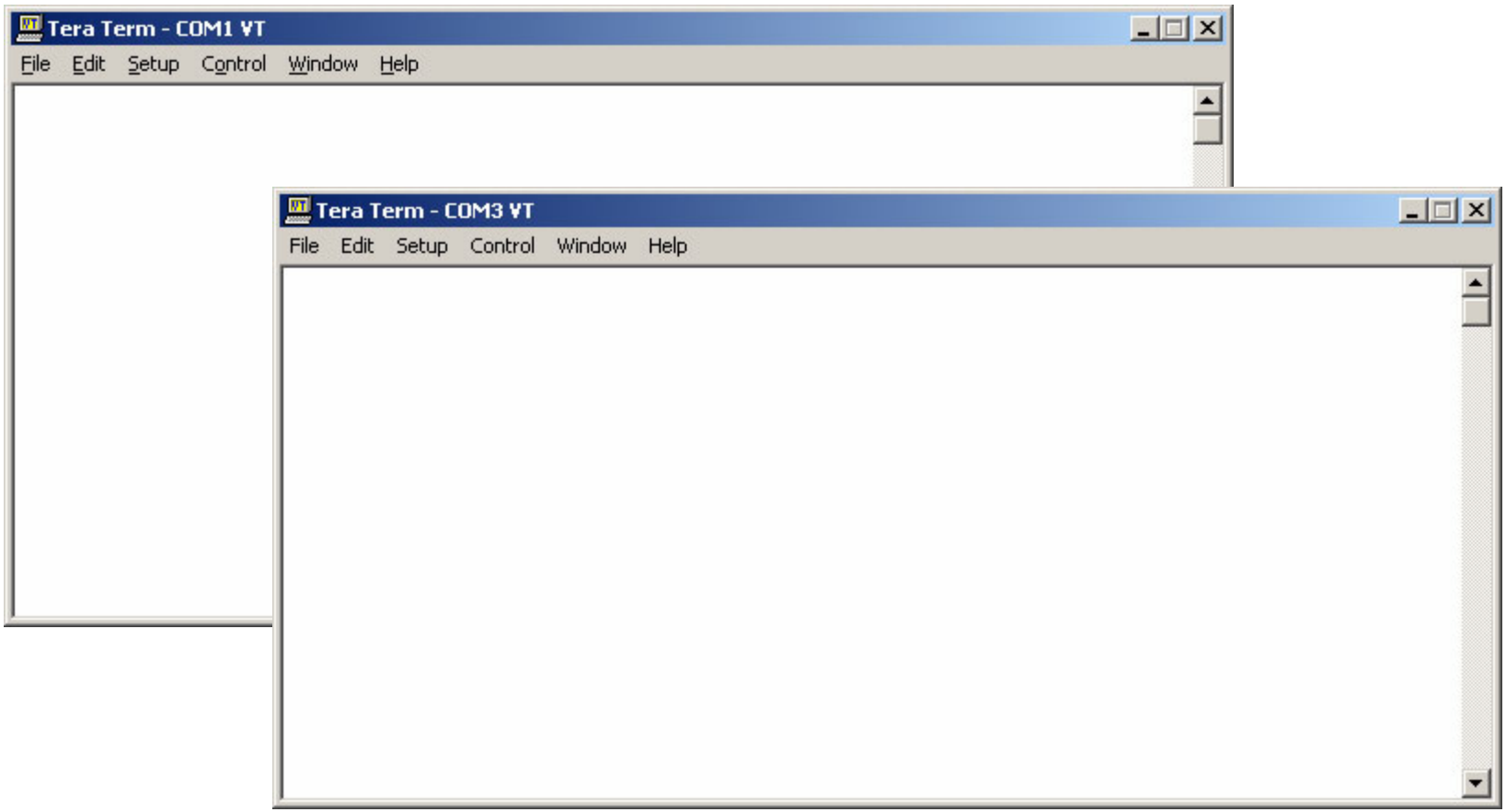
- Use a DVI/VGA adapter to connect a VGA monitor
  - http://www.belkin.com

Hardware Setup

- USB Keyboard
  - www.dell.com

Software Setup

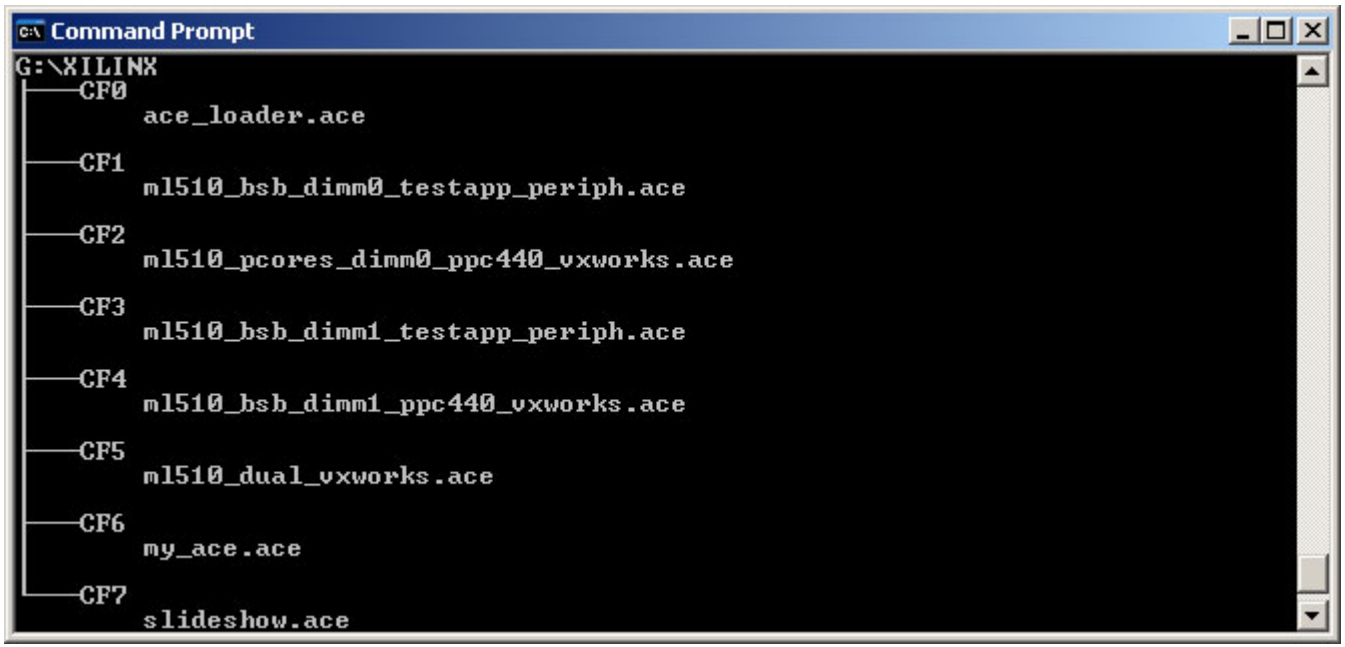
- Start a Terminal Program for each UART:



Note: Presentation applies to the ML510

Factory CompactFlash

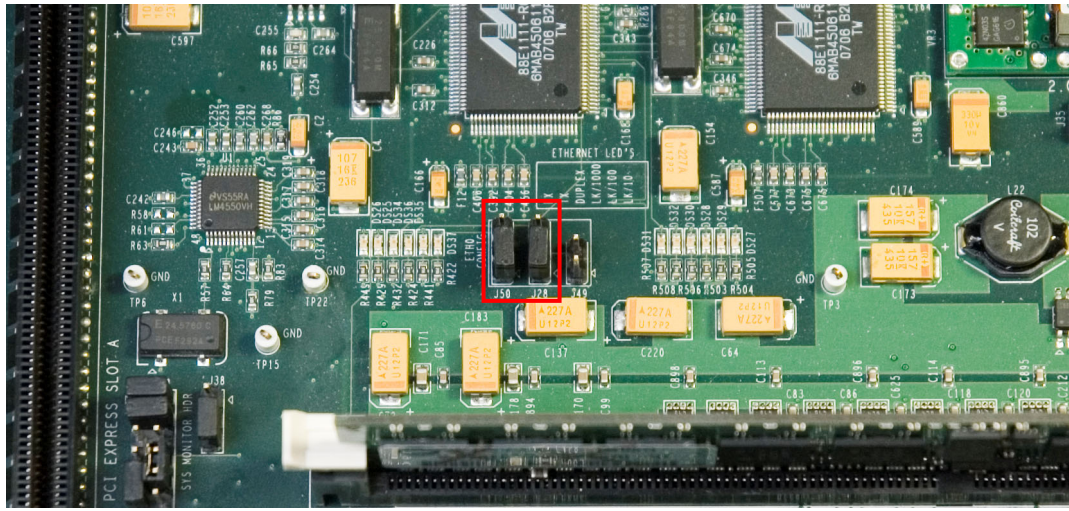
- The CompactFlash shipped with the ML510 board has the following ace files preloaded:



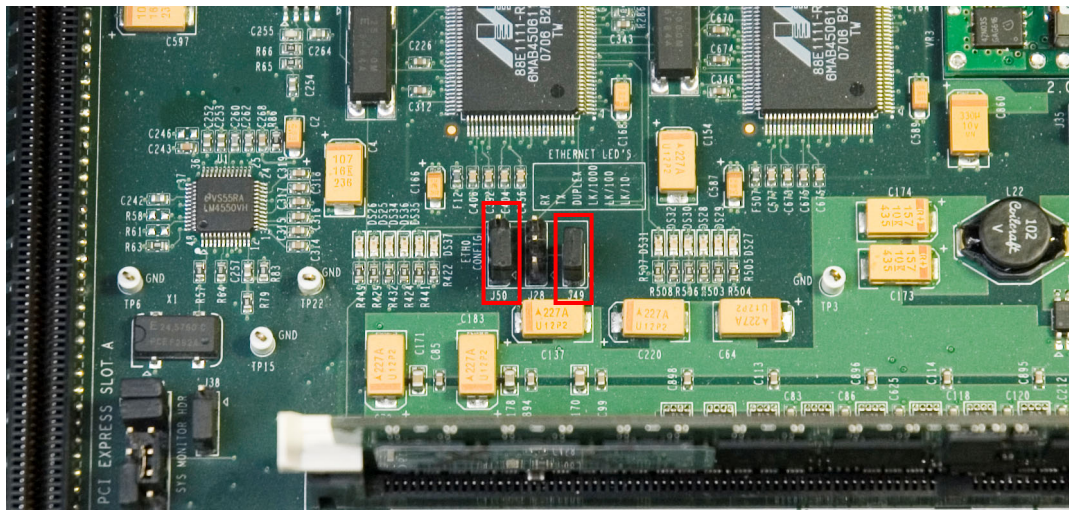
Note: Presentation applies to the ML510

Network Setup

- Set PHY0 Jumpers
- MII – Connect pins 1 & 2 on J50 and J28



- RGMII – Connect pins 1 & 2 on J50; connect J49



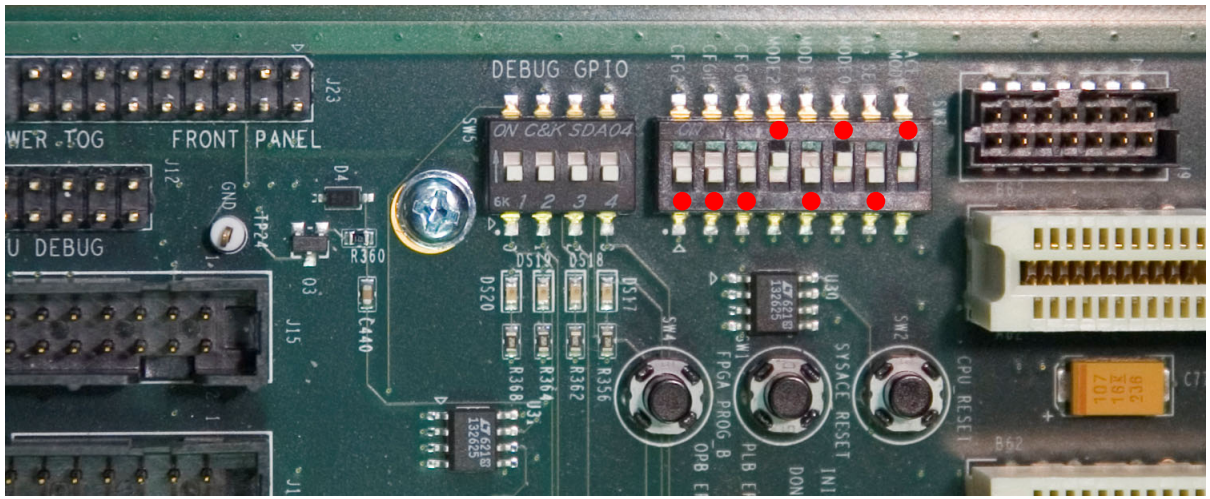
Note: Refer to the ML510 User Guide – UG356 for details

CompactFlash Setup

- Insert the CompactFlash provided with the ML510 fully into the CompactFlash slot on the ML510 board

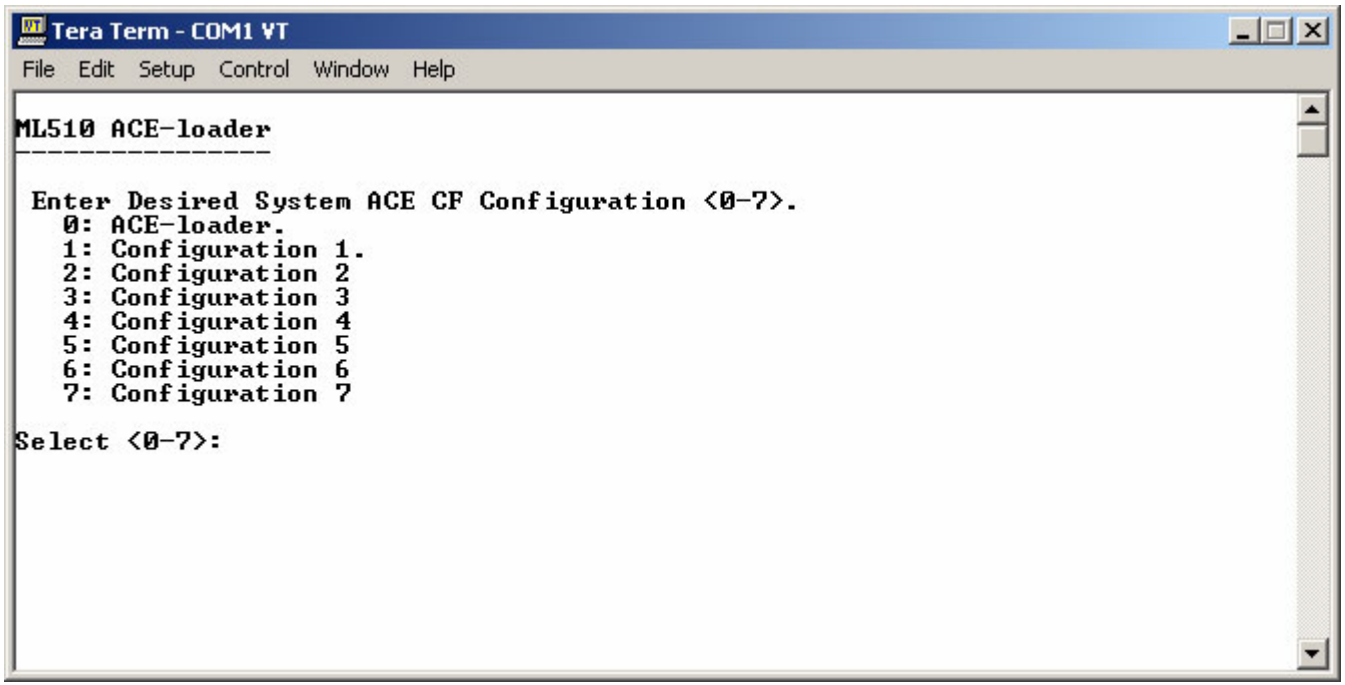
Equipment Setup

- Set SW3 DIP Switches to 00010101 (1 = ON)
- Power-up the ML510 board



ACE–Loader

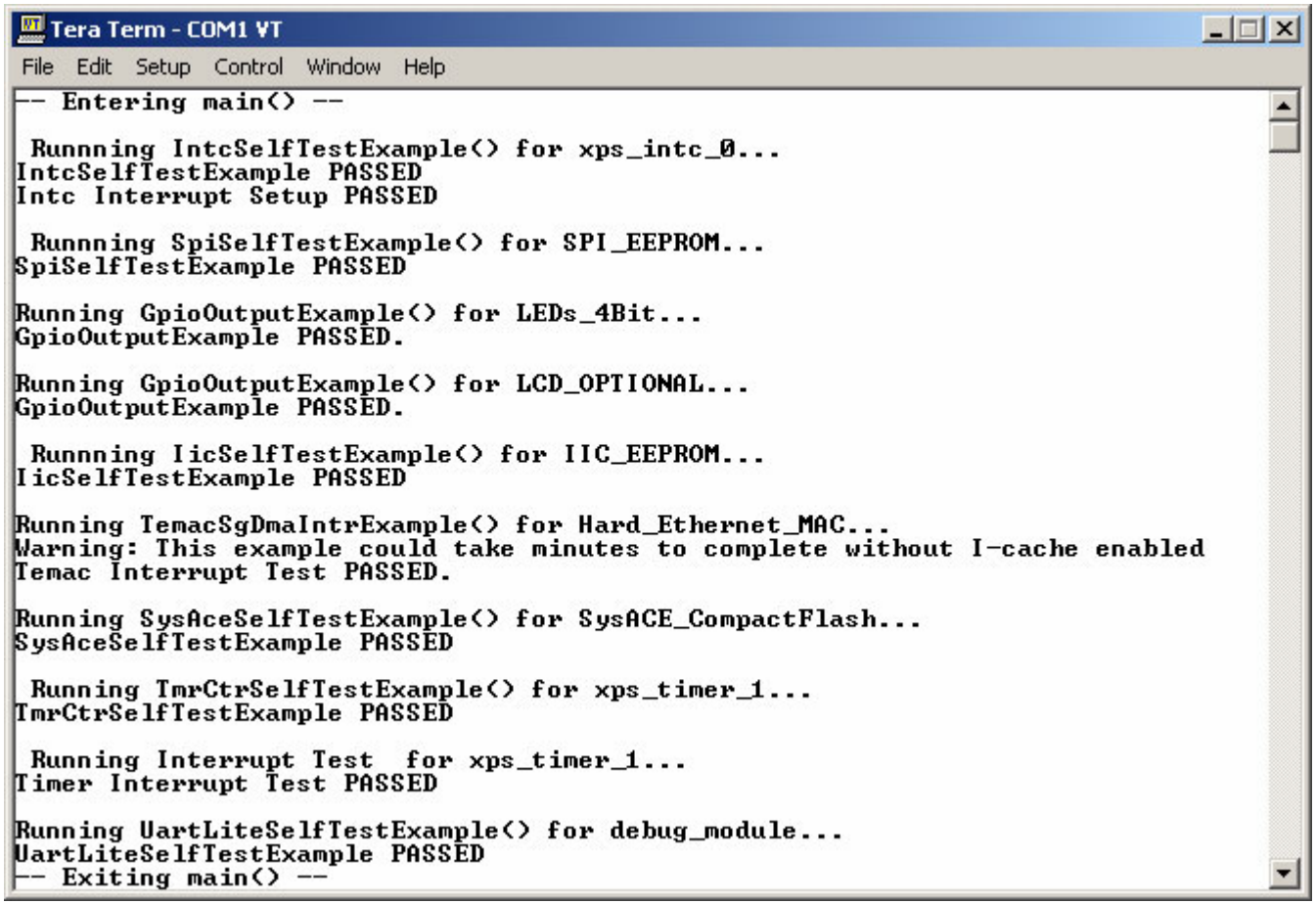
- The terminal window also reflects the ACE-loader application
- Type the desired number in the terminal window to choose an application
- After each demo, push the SysACE reset to return to bootload



Note: Presentation applies to the ML510

CF1 – TestApp Peripheral

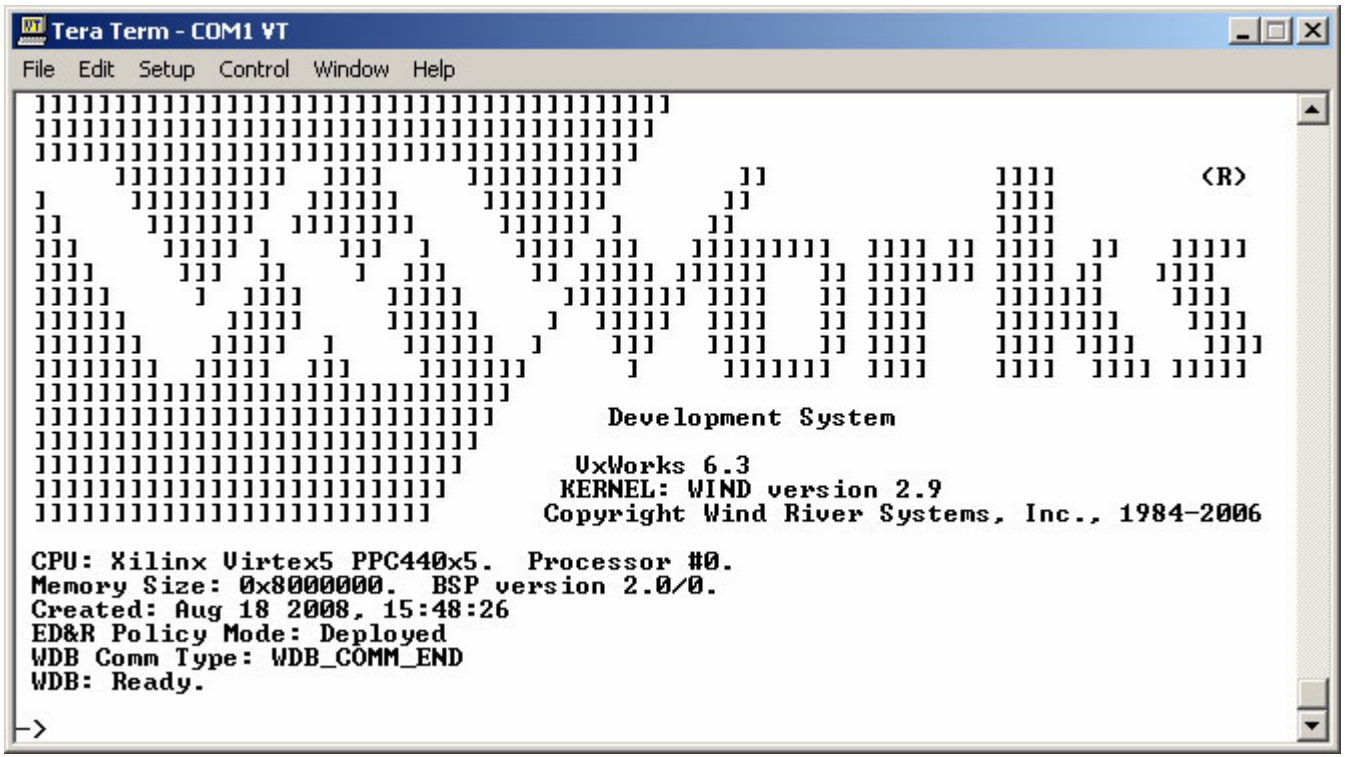
- Type 1, to launch the TestApp Peripheral DIMM0 design
  - Set jumpers for MII; takes several minutes to complete



Note: MicroBlaze DIMM0 Design

CF2 – VxWorks DIMM0

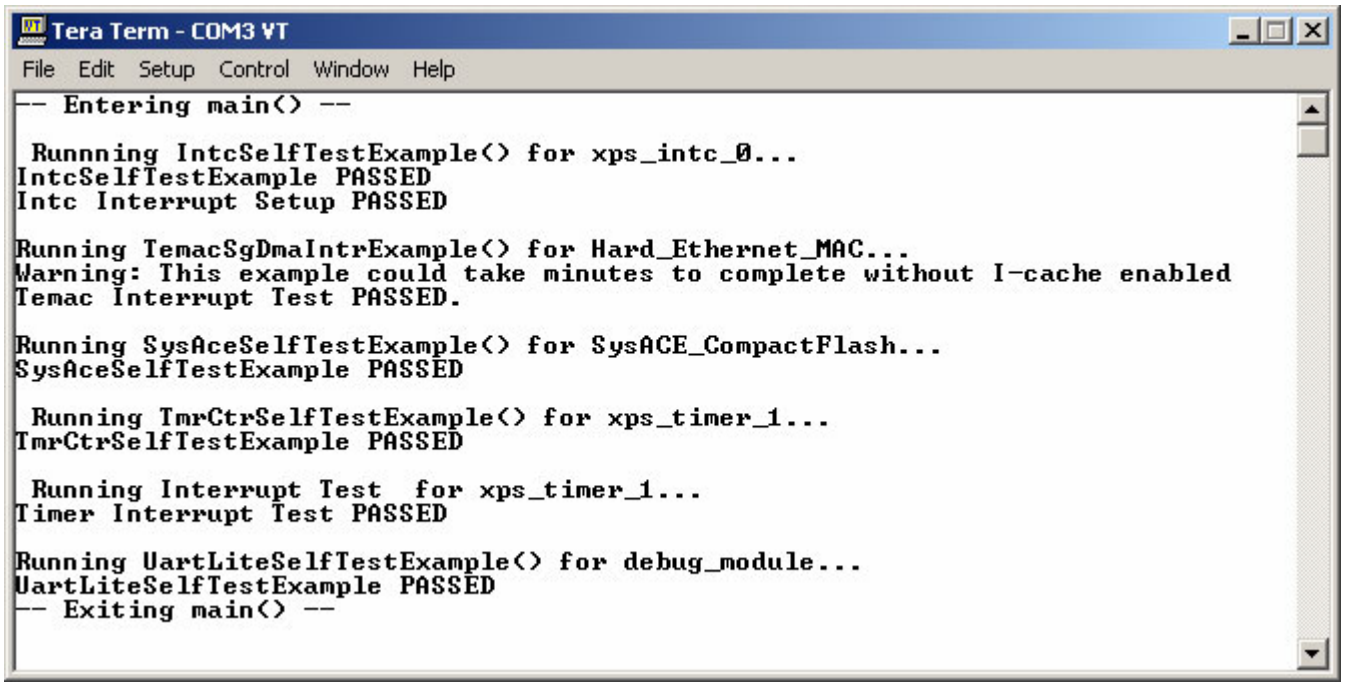
- Type 2, to launch the VxWorks on the Pcore DIMM0 design



Note: PPC440 DIMM0 Design

CF3 – TestApp Peripheral

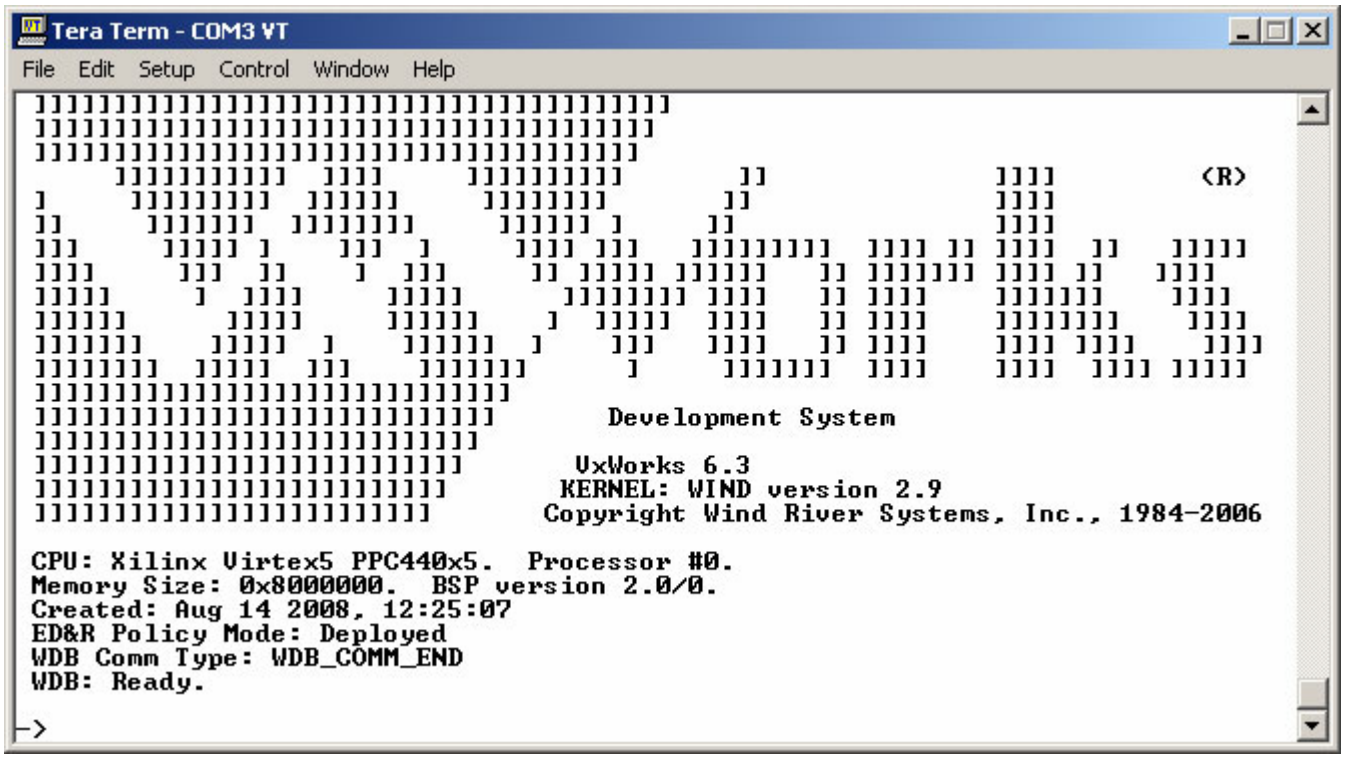
- Type 3, to launch the TestApp Peripheral DIMM1 design
  - View on COM2; takes several minutes to complete



Note: MicroBlaze DIMM1 Design

CF4 – VxWorks DIMM1

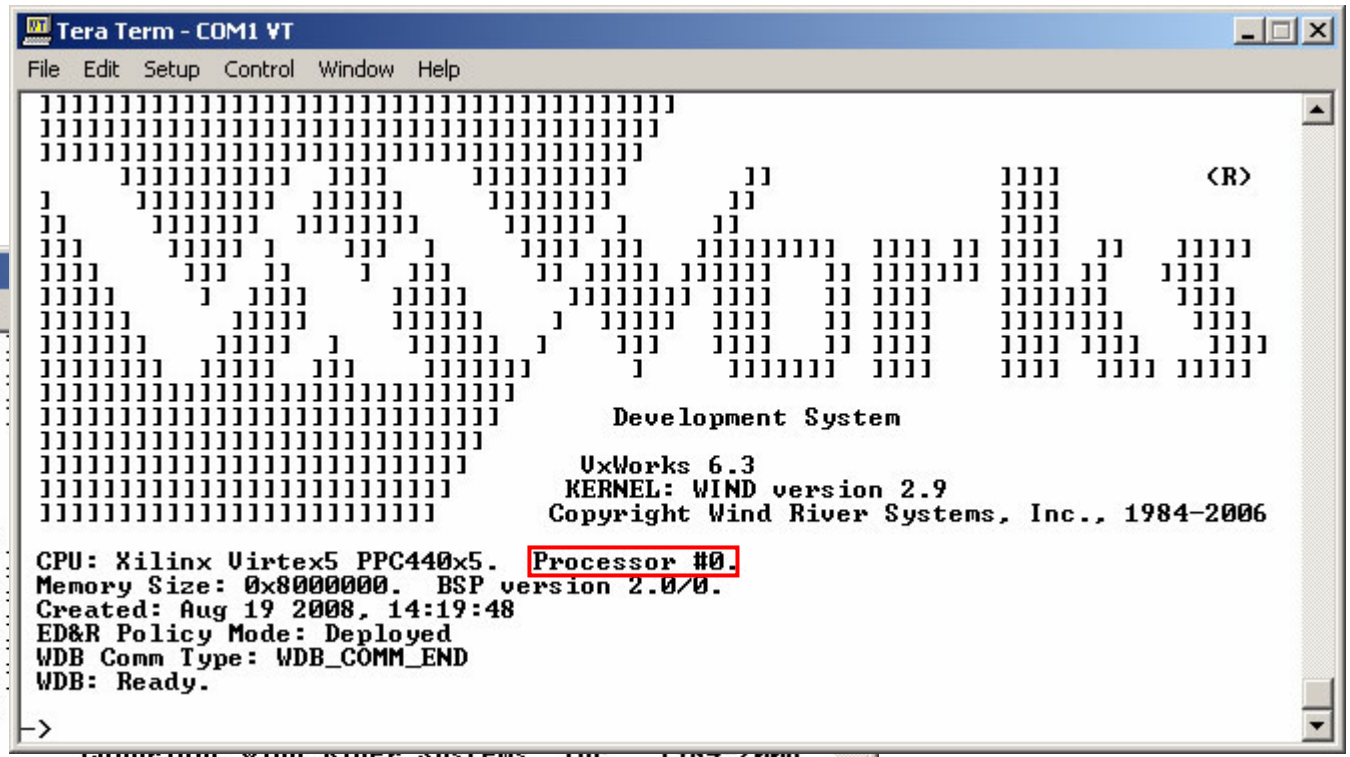
- Type 4, to launch the VxWorks on the BSB DIMM1 design

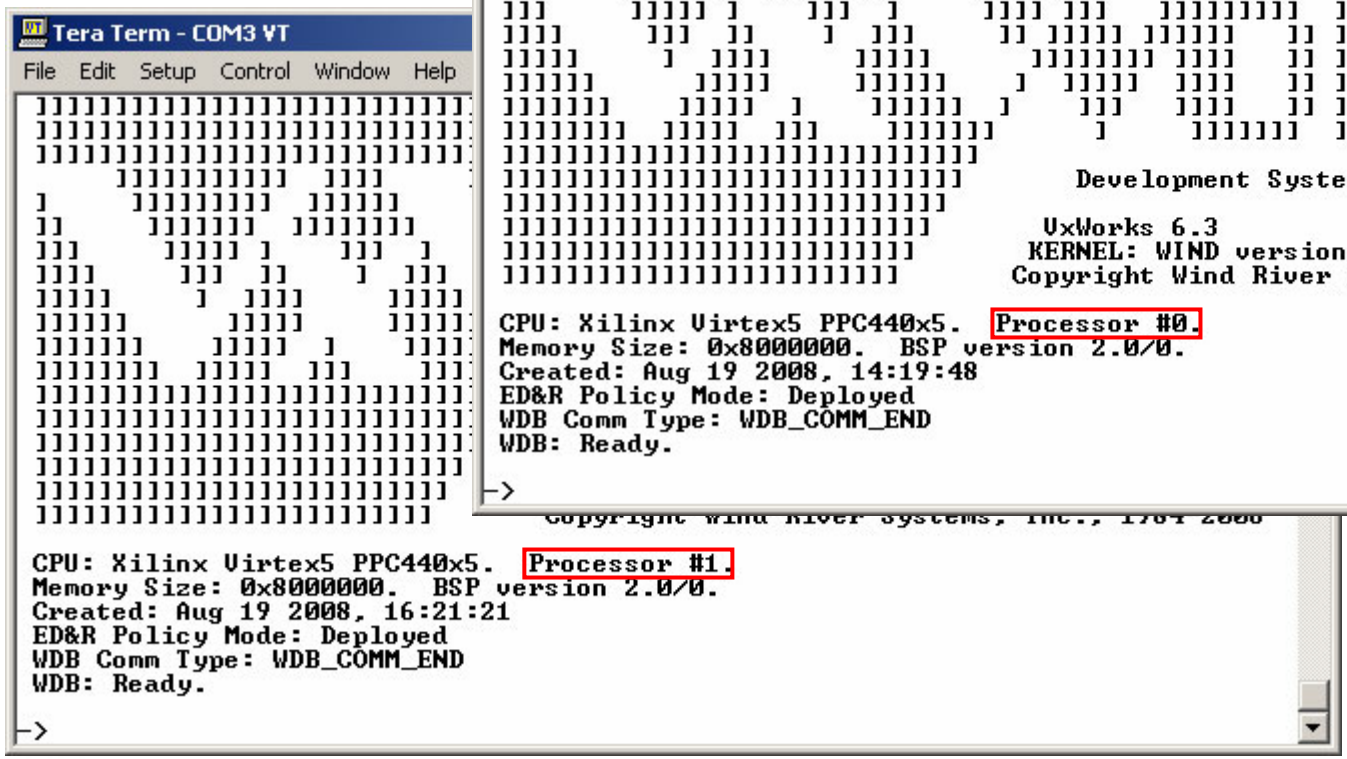


Note: PPC440 DIMM1 Design

CF5 – Dual VxWorks

- Type 5, to launch the Dual Processor VxWorks design
  - Set jumpers for RGMII

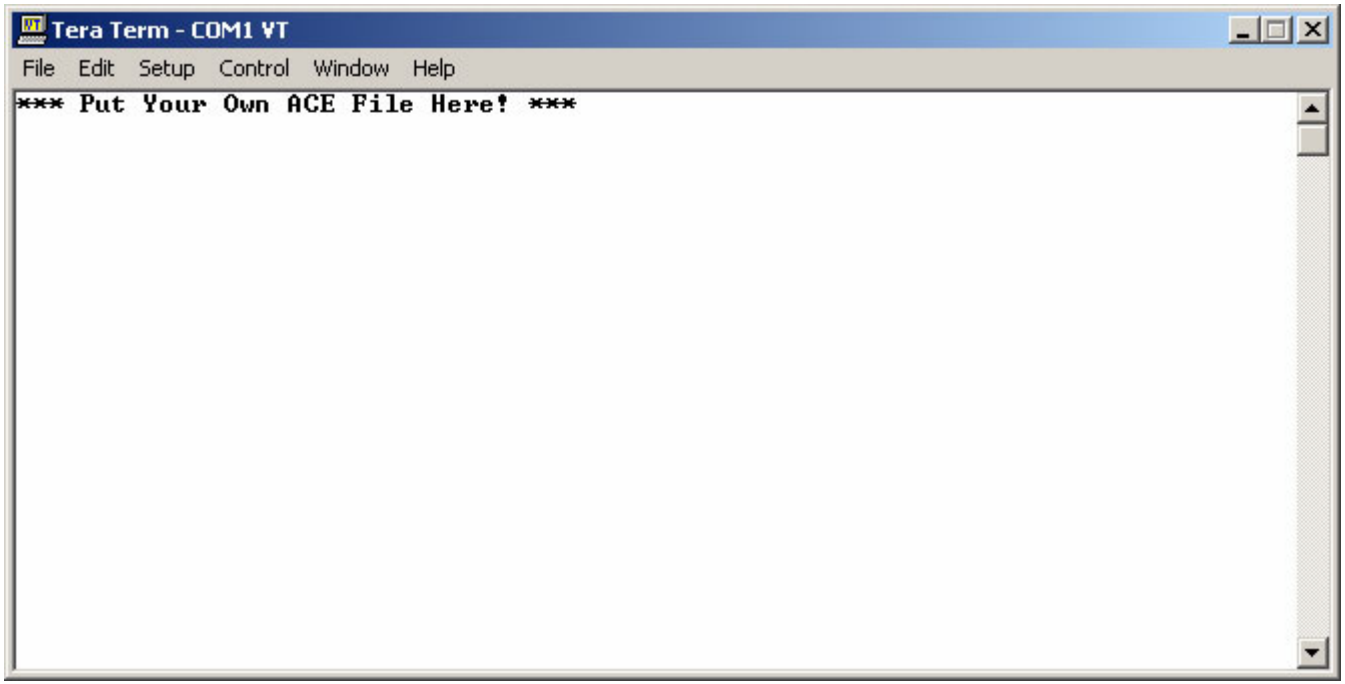




Note: Dual PPC440 Design

CF6 – My ACE

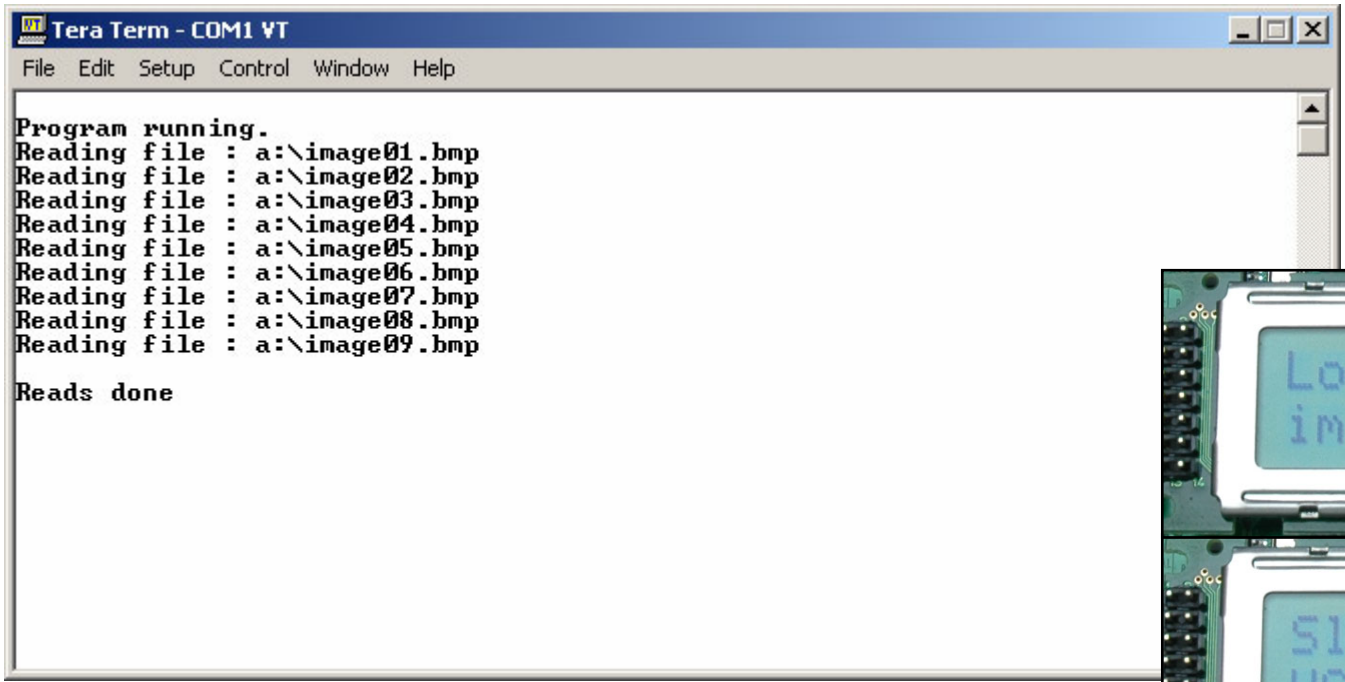
- Type 6, to launch the placeholder design, my_ace
  - Same message appears on the Monitor



Note: PPC440 Pcore DIMM0 Design

CF7 – Slideshow

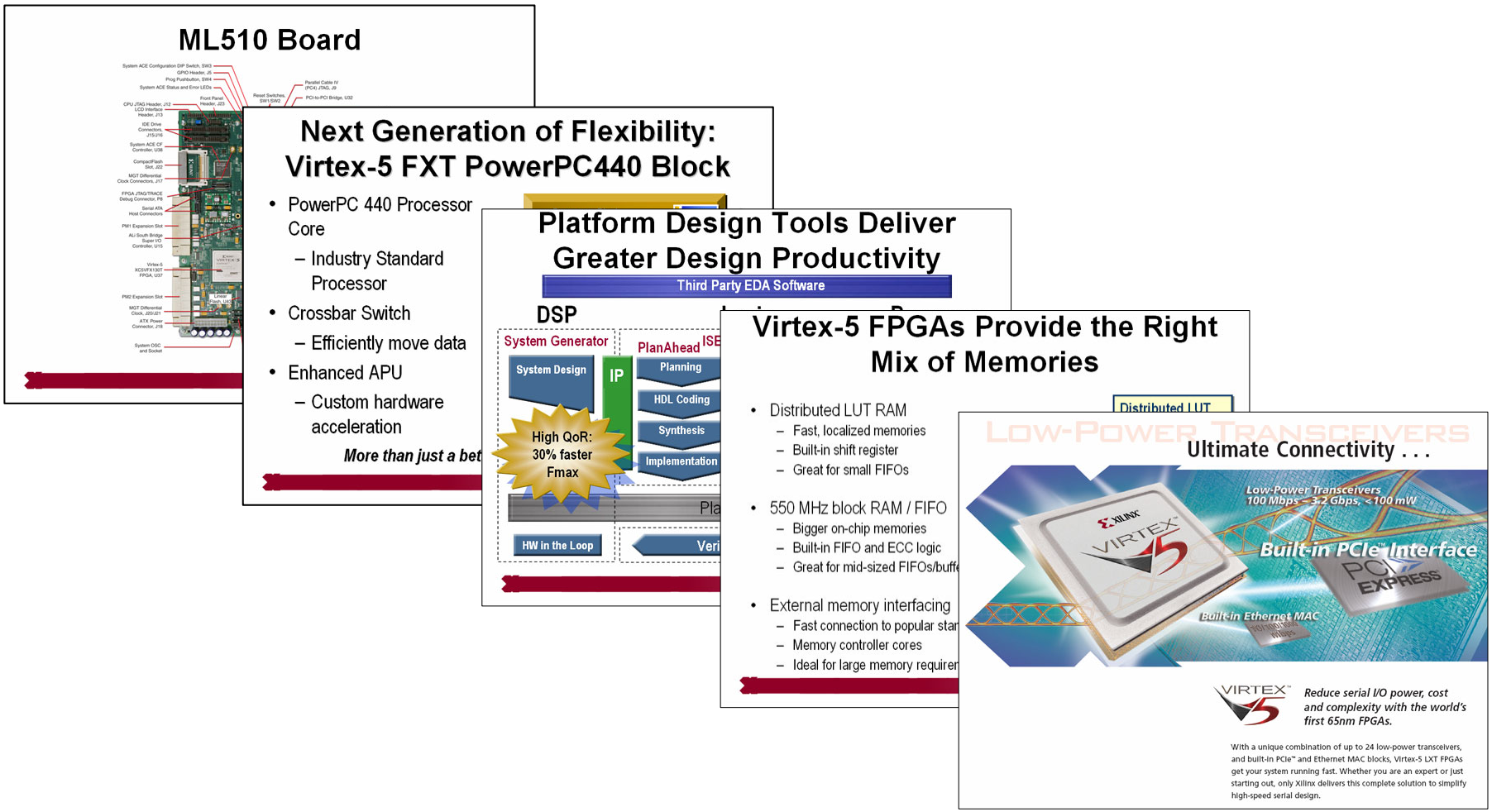
- Type 7, to launch the slideshow application
- The slideshow loads the presentation into memory then presents it



Note: Presentation applies to the ML510

Slideshow

- The slideshow app will present a series of slides on the Monitor:



Note: Presentation applies to the ML510

Documentation

- Virtex-5
  - Silicon Devices
    http://www.xilinx.com/products/silicon_solutions
  - Virtex-5 Multi-Platform FPGA
    http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms
    http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet
    http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf

Documentation

- Virtex-5
  - Virtex-5 FPGA User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
  - Virtex-5 FPGA Configuration User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
  - Virtex-5 System Monitor User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug192.pdf
  - Virtex-5 Packaging and Pinout Specification
    http://www.xilinx.com/support/documentation/user_guides/ug195.pdf

Documentation

- Virtex-5 RocketIO
  - RocketIO GTP Transceivers

    http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTP.htm
  - RocketIO GTX Transceivers

    http://www.xilinx.com/products/silicon_solutions/fpgas/virtex/virtex5/capabilities/RocketIO_GTX.htm
  - RocketIO GTP Transceiver User Guide – UG196

    http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
  - RocketIO GTX Transceiver User Guide – UG198

    http://www.xilinx.com/support/documentation/user_guides/ug198.pdf

Documentation

- Design Resources
  - ISE Development Tools and IP
    http://www.xilinx.com/ise
  - Integrated Software Environment (ISE) Foundation Resources
    http://www.xilinx.com/ise/logic_design_prod/foundation.htm
  - ISE Manuals
    http://www.xilinx.com/support/software_manuals.htm
  - ISE Development System Reference Guide
    http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf
  - ISE Development System Libraries Guide
    http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf

Documentation

- Additional Design Resources
  - Customer Support
    http://www.xilinx.com/support
  - Xilinx Design Services:
    http://www.xilinx.com/xds
  - Titanium Dedicated Engineering:
    http://www.xilinx.com/titanium
  - Education Services:
    http://www.xilinx.com/education
  - Xilinx On Board (Board and kit locator):
    http://www.xilinx.com/xob

Documentation

- Platform Studio
  - Embedded Development Kit (EDK) Resources
    http://www.xilinx.com/edk
  - Embedded System Tools Reference Manual
    http://www.xilinx.com/support/documentation/sw_manuals/edk10_est_rm.pdf
  - EDK Concepts, Tools, and Techniques
    http://www.xilinx.com/support/documentation/sw_manuals/edk_ctt.pdf

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Documentation

- PowerPC 440
  - PowerPC 440 Processor
    http://www.xilinx.com/powerpc
  - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200
    http://www.xilinx.com/support/documentation/user_guides/ug200.pdf
  - PPC440 Virtex-5 Wrapper – DS621
    http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf
  - DDR2 Memory Controller for PowerPC 440 Processors – DS567
    http://www.xilinx.com/support/documentation/data_sheets/ds567.pdf

Documentation

- MicroBlaze
  - MicroBlaze Processor
    http://www.xilinx.com/microblaze
  - MicroBlaze Processor Reference Guide – UG081
    http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf

Documentation

- Memory Solutions
  - Demos on Demand – Memory Interface Solutions with Xilinx FPGAs
    http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35
  - Xilinx Memory Corner
    http://www.xilinx.com/products/design_resources/mem_corner
  - Additional Memory Resources
    http://www.xilinx.com/support/software/memory/protected/index.htm
  - Xilinx Memory Interface Generator (MIG) 2.2 User Guide
    http://www.xilinx.com/support/documentation/ip_documentation/ug086.pdf
  - Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator
    http://www.xilinx.com/support/documentation/white_papers/wp260.pdf

Documentation

- ChipScope Pro
  - ChipScope Pro 10.1i Serial IO Toolkit User Manual
    http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf
  - ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide
    http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf

Documentation

- Ethernet
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf
  - Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide
    http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf
  - Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide
    http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
  - LightWeight IP (lwIP) Application Examples – XAPP1026
    http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf

Documentation

- PLB v4.6 IP
  - Processor Local Bus (PLB) v4.6 Data Sheet – DS531
    http://www.xilinx.com/support/documentation/ip_documentation/plb_v46.pdf
  - Multi-Port Memory Controller (MPMC) – DS643
    http://www.xilinx.com/support/documentation/ip_documentation/mpmc.pdf
  - XPS Multi-CHannel External Memory Controller (XPS MCH EMC) – DS575
    http://www.xilinx.com/support/documentation/ip_documentation/xps_mch_emc.pdf
  - XPS LocalLink TEMAC – DS537
    http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_temac.pdf
  - XPS LocalLink FIFO – DS568
    http://www.xilinx.com/support/documentation/ip_documentation/xps_ll_fifo.pdf

Documentation

- PLB v4.6 IP
  - XPS IIC Bus Interface – DS606
    http://www.xilinx.com/support/documentation/ip_documentation/xps_iic.pdf
  - XPS SYSACE (System ACE) Interface Controller – DS583
    http://www.xilinx.com/support/documentation/ip_documentation/xps_sysace.pdf
  - XPS Timer/Counter – DS573
    http://www.xilinx.com/support/documentation/ip_documentation/xps_timer.pdf
  - XPS Interrupt Controller – DS572
    http://www.xilinx.com/support/documentation/ip_documentation/xps_intc.pdf
  - Using and Creating Interrupt-Based Systems Application Note
    http://www.xilinx.com/support/documentation/application_notes/xapp778.pdf

Documentation

- PLB v4.6 IP
  - XPS General Purpose Input/Output (GPIO) – DS569
    http://www.xilinx.com/support/documentation/ip_documentation/xps_gpio.pdf
  - XPS External Peripheral Controller (EPC) – DS581
    http://www.xilinx.com/support/documentation/ip_documentation/xps_epc.pdf
  - XPS 16550 UART – DS577
    http://www.xilinx.com/support/documentation/ip_documentation/xps_uart16550.pdf
  - PLBV46 to DCR Bridge Data Sheet – DS578
    http://www.xilinx.com/support/documentation/ip_documentation/plbv46_dcr_bridge.pdf

Documentation

- IP
  - Local Memory Bus Data Sheet – DS445
    http://www.xilinx.com/support/documentation/ip_documentation/lmb_v10.pdf
  - Block RAM Block Data Sheet – DS444
    http://www.xilinx.com/support/documentation/ip_documentation/bram_block.pdf
  - Microprocessor Debug Module Data Sheet – DS641
    http://www.xilinx.com/support/documentation/ip_documentation/mdm.pdf
  - LMB Block RAM Interface Controller Data Sheet – DS452
    http://www.xilinx.com/support/documentation/ip_documentation/lmb_bram_if_cntlr.pdf
  - Device Control Register Bus (DCR) v2.9 Data Sheet – DS406
    http://www.xilinx.com/support/documentation/ip_documentation/dcr_v29.pdf

Documentation

- IP
  - JTAGPPC Controller Data Sheet – DS298
    http://www.xilinx.com/support/documentation/ip_documentation/jtagppc_cntlr.pdf
  - Processor System Reset Module Data Sheet – DS402
    http://www.xilinx.com/support/documentation/ip_documentation/proc_sys_reset.pdf
  - Clock Generator v2.0 Data Sheet – DS614
    http://www.xilinx.com/support/documentation/ip_documentation/clock_generator.pdf
  - Util Bus Split Operation Data Sheet – DS484
    http://www.xilinx.com/support/documentation/ip_documentation/util_bus_split.pdf

Documentation

- ML510
  - ML510 Overview
    http://www.xilinx.com/ml510
  - ML510 Evaluation Platform User Guide – UG356
    http://www.xilinx.com/support/documentation/boards_and_kits/ug356.pdf
  - ML510 Reference Design User Guide – UG355
    http://www.xilinx.com/support/documentation/boards_and_kits/ug355.pdf
  - ML510 Quickstart Tutorial
    http://www.xilinx.com/products/boards/ml510/docs/ml510_quickstart.pdf

Documentation

- ML510
  - ML510 Schematics

    http://www.xilinx.com/support/documentation/boards_and_kits/ml510_schematics.pdf
  - ML510 Bill of Material

    http://www.xilinx.com/support/documentation/boards_and_kits/ml510_bom.xls