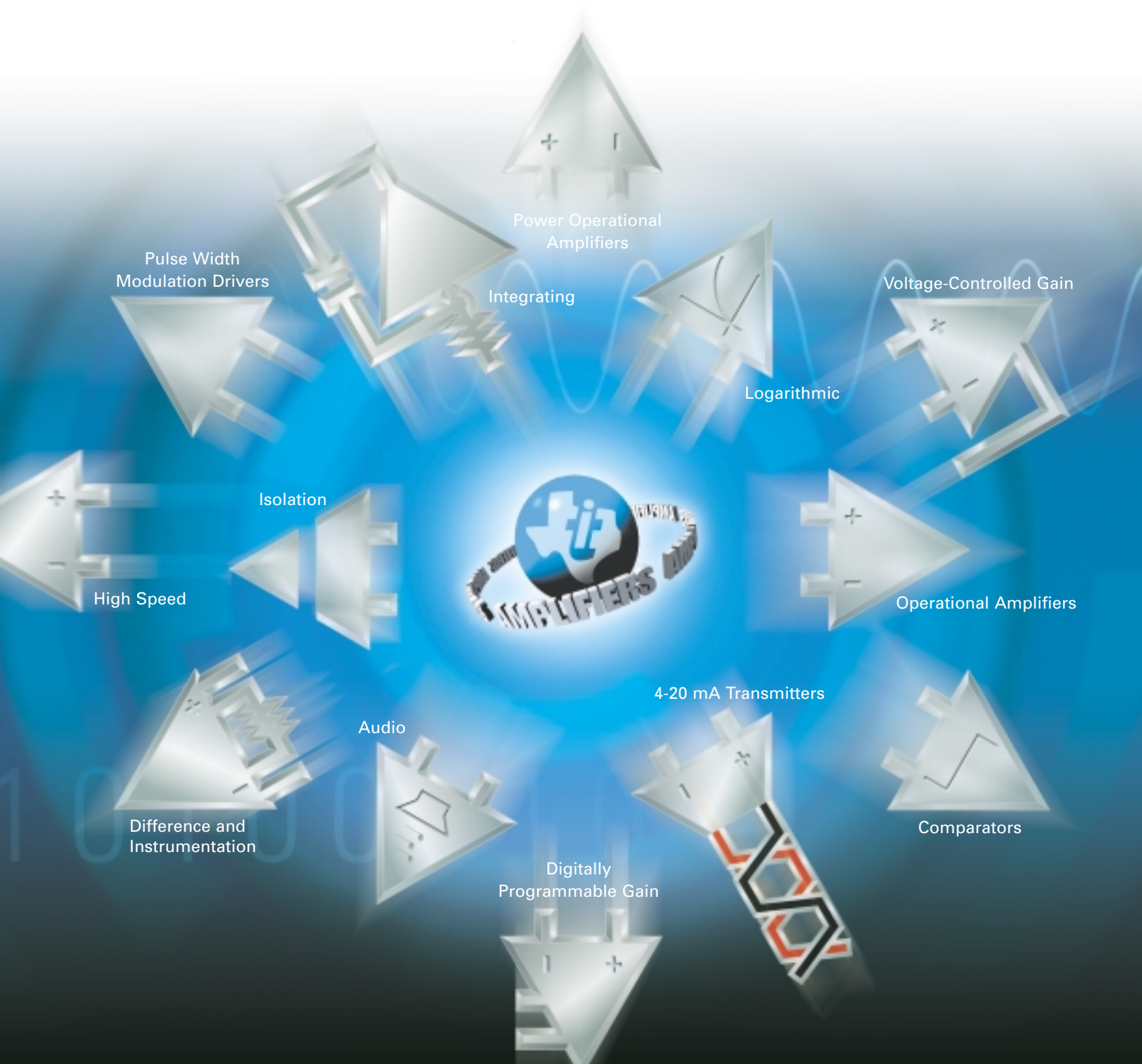


# Amplifier Selection Guide

1Q 2003

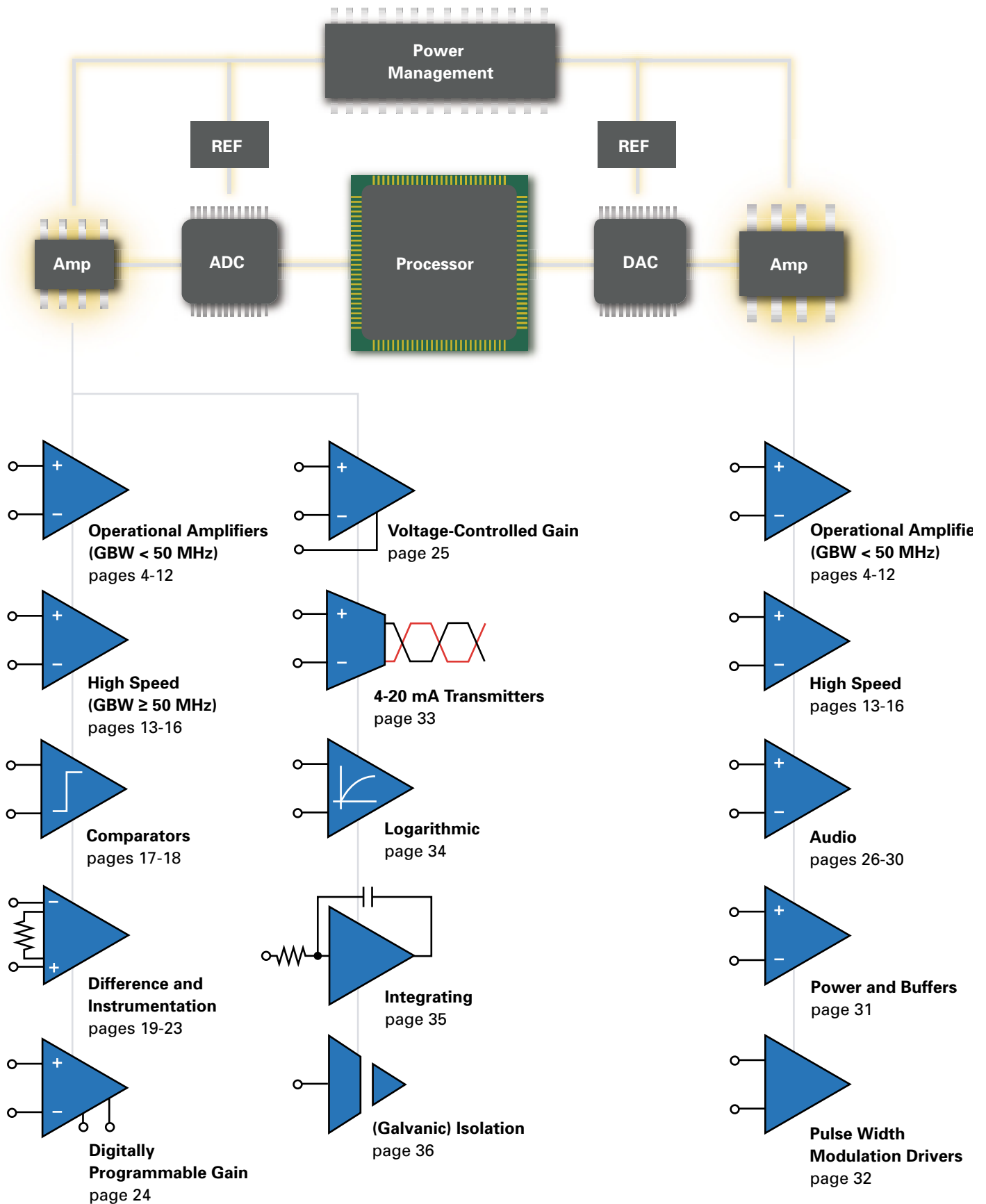


Includes



**Burr-Brown Products**  
from Texas Instruments

# Amplifier Selection Tree



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Texas Instruments offers a wide range of amplifiers that vary in performance, functionality and technology. Whether your design requires low-noise, high-precision or low-voltage micropower signal conditioning, TI's amplifier portfolio will meet your requirements and with a variety of micropackage options.

## Why TI Amplifiers?

- High performance—maximum performance, minimum power.
- Largest portfolio of op amps in the industry.
- Cost-efficient signal conditioning solutions.
- Maximize your signal chain performance.


## TI offers devices useful anywhere analog applications require:

- High reliability
- Precision
- Wide dynamic range
- Wide bandwidth
- Wide temperature range
- Stability over time

## Recently Released Products

- [OPA363](#)—1.8 V, RRIO, low noise, excellent CMRR.
- [OPA335](#)—zero-drift, low-power, CMOS amplifier.
- [OPA354](#)—100-MHz, RRIO, CMOS amplifier family.
- [OPA356](#)—200-MHz, RRO, CMOS amplifier family.
- [OPA348](#)—1-MHz, 45- $\mu$ A, RRIO, CMOS amplifier family.
- SC70 package now available for [OPA348](#), [OPA349](#), [OPA347](#).
- [TPA2005](#)—1.1-W, mono, Class-D, filter-free, audio power amplifier.
- [LOG2112](#)—dual version of the LOG112 with 7.5 decades of dynamic range.
- [TLV349x](#)—1.8-V, high-speed, low-power, push-pull comparator.
- [INA330](#)—thermistor signal amp for temperature control.

# Operational Amplifiers

 Texas Instruments offers a wide range of op amp types including high precision, micropower, low voltage, high speed and rail-to-rail in several different process technologies. TI has developed the industry's largest selection of low power and low voltage op amps with features designed to satisfy a very wide range of applications. To help facilitate the selection process, an interactive online op amp parametric search engine is available at [amplifier.ti.com/search](http://amplifier.ti.com/search) with links to all op amp specifications.

## Design Considerations

Choosing the best op amp for an application involves consideration of a variety of interrelated requirements. In doing so, designers must trade-off often conflicting size, cost and performance objectives. Even experienced engineers can find the task daunting but it need not be. Keeping in mind the following issues, the choice can quickly be narrowed to a manageable few.

**Supply voltage ( $V_S$ )**—tables include low-voltage ( $< 2.7\text{ V min}$ ) and wide voltage range ( $> 5\text{ V min}$ ) sections. Other op amp selection criteria (e.g. precision) can be quickly examined in the supply range column for an appropriate choice. Applications operating from a single power supply may require rail-to-rail performance and consideration of precision-related parameters.

**Precision**—primarily associated with input offset voltage ( $V_{OS}$ ) and its change with respect to temperature drift, PSRR

## Common Op Amp Design Questions

**What is the amplitude of the input signal?** To ensure that signal errors are small relative to the input signal, small input signals require high precision, (e.g. low offset voltage) amplifiers. Ensure that the amplified output signal stays within the amplifier output voltage.

**Will the ambient temperature vary?** Op amps are sensitive to temperature variations, so it is often to consider offset voltage drift over temperature.

**Does the common-mode voltage vary?** Make sure the op amp is operated within its common-mode range and has an adequate common-mode rejection ratio (CMRR). Common-mode voltage will induce additional offset voltage.

**Does the power supply voltage vary?** Power supply variations affect the offset voltage. This may be especially important in battery-powered applications.

### Precision Application Examples

- High gain circuits ( $G > 100$ )
- Measuring small input signals (i.e. from a thermocouple)
- Wide operating temperature range circuits (i.e. in automotive or industrial applications)
- Single-supply  $\leq 5\text{-V}$  data-acquisition systems where input voltage span is limited

and CMRR. It is generally used to describe op amps with low input offset voltage and low input offset voltage temperature drift. Precision op amps are required when amplifying tiny signals from thermocouples and other low-level sensors. High-gain or multi-stage circuits may require low offset voltage.

**Gain-bandwidth product (GBW)**—the gain bandwidth of a voltage-feedback op amp determines its useful bandwidth in an application. The available bandwidth is approximately equal to the gain bandwidth divided by the closed-loop gain of the application. For voltage feedback amplifiers, GBW is a constant. Many applications

require much wider bandwidth to achieve low distortion, excellent linearity, good gain accuracy, gain flatness or other behavior that is influenced by feedback factors.

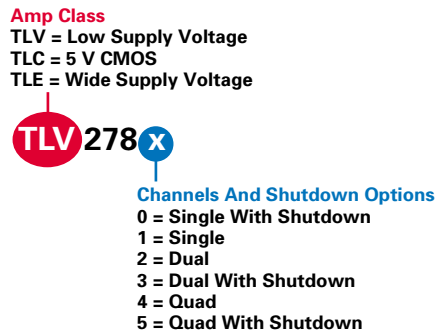
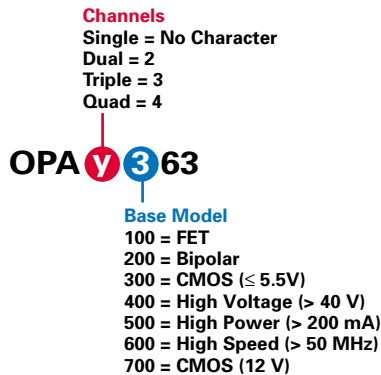
**Power ( $I_Q$  requirements)**—a significant issue in many applications. Because op amps can have a considerable impact on the overall system power budget, quiescent current, especially in battery-powered applications, is a key design consideration.

**Rail-to-rail performance**—rail-to-rail output provides maximum output voltage swing for widest dynamic range. This may be particularly important with low operating

Supply Voltage	Design Requirements	Typical Applications	Recommended Process	Recommended TI Amp Family
$V_S \leq 5\text{ V}$	Rail-to-Rail, Low Power, Precision, Small Packages	Battery-Powered, Handheld	CMOS	OPA3xx, TLVxxxx
$V_S \leq 16\text{ V}$	Rail-to-Rail, Low Noise, Low Voltage Offset, Precision, Small Packages	Industrial, Automotive	CMOS	OPA3x, TLCxxxx, OPA7xx
$V_S \leq +36\text{ V}$	Low Input Bias Current, Low Offset Current, High Input Impedance	Industrial, Test Equipment, ONET, High-end Audio	FET, DiFET	OPA1xx, OPA627
$V_S \leq +44\text{ V}$	Low Voltage Offset, Low Drift	Industrial, Test Equipment, ONET, High-end Audio	Bipolar	OPA2xx, TLExxxx
$\pm 5\text{ V to } \pm 15\text{ V}$ Dual Supply	High Speed on Dual Supplies	XDSL, Video, Professional Imaging, Data Converter Signal Conditioning	DiFET, High-Speed Bipolar, BiCOM	OPA6xx*, THSxxxx*
$2.7\text{ V} \leq V_S \leq 5\text{ V}$ Single Supply	High Speed on Single Supply	Consumer Imaging, Data Converter Signal Conditioning, Safety-Critical Automotive	High-Speed CMOS	OPA35x, OPA6xx*, THSxxxx*

\*See high-speed section, page 13.

## Op Amp Naming Conventions



voltage where signal swings are limited. Rail-to-rail input capability is often required to achieve maximum signal swing in buffer ( $G = 1$ ) single-supply applications. It can be useful in other applications, depending on amplifier gain and biasing considerations.

**Voltage noise ( $V_n$ )**—amplifier-generated noise may limit the ultimate dynamic range, accuracy or resolution of a system. Low-noise op amps can improve accuracy even in slow DC measurements.

**Input bias current ( $I_B$ )**—can create offset error by reacting with source or feedback impedances. Applications with high source impedance or high impedance feedback elements (such as transimpedance amplifiers or integrators) often require low input bias current. FET-input and CMOS op amps generally provide very low input bias current.

**Slew rate**—the maximum rate of change of the amplifier output. It is important when driving large signals to high frequency.

**Package size**—TI offers a wide variety of micropackages, including SOT23 and SC70 and small, high power-dissipating PowerPAD™ packages to meet space-sensitive and high-output drive requirements. Many TI single channel op amps are available in SOT23, with some dual amplifiers in SOT23-8.

**Shutdown mode**—an enable/disable function that places the amp in a high impedance state, reducing quiescent current in many cases to less than 1  $\mu A$ . Allows designers to use wide bandwidth op amps in lower power apps.

**Decompensated amplifiers**—for applications with gain greater than unity gain ( $G = 1$ ), decompensated amps provide significantly higher bandwidth, improved slew rate and lower distortion over their unity-gain stable counterparts on the same quiescent current or noise.

## Op Amp Rapid Selector

The tables on the following pages have been divided and subdivided into several categories to help quickly narrow the alternatives.

**Precision**  $V_{OS} \leq 500 \mu V$   
 Low Noise . . . . . pg 6  
 $V_N \leq 10nV/\sqrt{Hz}$   
 Low Voltage . . . . . pg 6  
 $V_S \leq 2.7 V$   
 Low Power . . . . . pg 6  
 $I_Q \leq 1 mA/ch$   
 Low Input Bias Current . . . . . pgs 6-7  
 $I_B \leq 100 pA$   
 Wide Bandwidth . . . . . pg 7  
 $GBW \geq 5 MHz$

**Low Voltage**  $V_S \leq 2.7 V$   
 Low Input Bias Current . . . . . pg 7  
 $I_B \leq 100 pA$   
 Low Power . . . . . pg 8  
 $I_Q \leq 1 mA/ch$   
 Wide Gain Bandwidth . . . . . pg 8  
 $GBW \geq 5 MHz$

**Low Power**  $I_Q \leq 1 mA/ch$   
 Low Voltage . . . . . pg 9  
 $V_S \leq 2.7 V$   
 Wide Bandwidth . . . . . pg 9  
 $GBW \geq 5 MHz$

**Wide Voltage**  $\pm 5 V \leq V_S \leq \pm 20 V$   
 Precision . . . . . pg 10  
 $V_{OS} \leq 500 \mu V$   
 Low Power . . . . . pgs 10-11  
 $I_Q \leq 1 mA/ch$   
 Low Input Bias Current . . . . . pg 11  
 $I_B \leq 100 pA$   
 Wide Bandwidth . . . . . pg 11  
 $GBW \geq 5 MHz$

**General Purpose** . . . . . pg 11



## Precision Operational Amplifiers ( $V_{OS} \leq 500 \mu V$ ) Selection Guide

Device <sup>1</sup>	Description	Ch.	$V_S$ (V) (min)	$V_S$ (V) (max)	$I_Q$ Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	$V_{OS}$ (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	$I_B$ (pA) (max)	CMRR (dB) (min)	$V_N$ at 1 kHz (nV/ $\sqrt$ Hz) (typ)	Single Supply	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Precision, Low Noise <math>V_N \leq 10</math> nV/<math>\sqrt</math>Hz (typ) at 1 kHz</b>																
OPAy277	High Precision, Low Power	1, 2, 4	4	36	0.825	1	0.8	0.02	0.1	1000	130	8	N	N	PDIP, SOIC	0.92
OPAy227	Precision, Ultra-Low Noise	1, 2, 4	5	36	3.8	8	2.3	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
OPAy228	Precision, Low Noise, $G \geq 5$	1, 2, 4	5	36	3.8	33	10	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
TLE2027	Precision, Low Noise, Wide Bandwidth, Wide $V_S$	1	8	38	5.3	13	2.8	0.1	0.4	90000	100	2.5	N	N	SOIC	0.83
OPA627	Ultra-Low THD+N, DiFET Wide Bandwidth, Precision	1	9	36	7.5	16	55	0.1	0.4	5	106	5.2	N	N	PDIP, SOIC, TO-99	9.63
OPA637	Decompensated OPA627	1	9	36	7.5	80	135	0.1	0.4	5	106	4.5	N	N	PDIP, SOIC, TO-99	9.63
OPAy350	CMOS, 38 MHz	1, 2, 4	2.7	5.5	7.5	38	22	0.5	4	10	76	5	Y	I/O	PDIP, MSOP, SOIC, SSOP	1.23
TLC220x	Precision, Low Noise	1, 2	4.6	16	1.5	1.8	2.5	0.5	0.5	100	85	8	Y	Out	PDIP, SOIC	1.55
OPAy132	Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	4.8	8	20	0.5	2	50	96	8	N	N	PDIP, SOIC	1.35
<b>Precision, Low Voltage <math>V_S \leq 2.7</math> V (min)</b>																
<b>OPAy334</b>	Zero Drift, Precision, CMOS, Shutdown	1, 2	2.7	5.5	0.35	2	1.6	0.005	0.02	200	110	—	Y	Out	MSOP, SOIC, SOT23	0.95
<b>OPAy335</b>	Zero Drift, Precision, CMOS	1, 2	2.7	5.5	0.35	2	1.6	0.005	0.02	200	110	—	Y	Out	MSOP, SOIC, SOT23	0.95
OPAy234	Low Power, Precision	1, 2, 4	2.7	36	0.3	0.35	0.2	0.1	0.5	25000	96	25	Y	N	MSOP, SOIC	0.99
OPAy336	CMOS, $\mu$ Power	1, 2, 4	2.3	5.5	0.032	0.1	0.03	0.125	1.5	10	80	40	Y	Out	MSOP, PDIP, SOIC, SOT23	0.61
OPAy241	Bipolar, $\mu$ Power, High CMRR	1, 2, 4	2.7	36	0.025	0.35	0.1	0.25	0.4	2000	124	45	Y	Out	PDIP, SOIC	1.07
TLC1078	Low Voltage, Precision	2	1.4	16	0.017	0.085	0.032	0.45	1.1	70	600	68	N	—	SOIC, SOP, PDIP	2.17
OPAy340	CMOS, Wide Bandwidth	1, 2, 4	2.7	5.5	0.95	5.5	6	0.5	2.5	10	80	25	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy350	CMOS, 38 MHz	1, 2, 4	2.7	5.5	7.5	38	22	0.5	4	10	76	5	Y	I/O	PDIP, MSOP, SOIC, SSOP	1.23
<b>OPAy363</b>	1.8 V, High CMRR, SHDN	1, 2	1.8	5.5	0.75	7	5	0.5	2	10	74	17	Y	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR	1, 2, 4	1.8	5.5	0.75	7	5	0.5	2	10	74	17	Y	I/O	MSOP, SOIC, SOT23, TSSOP	0.55
<b>Precision, Low Power <math>I_Q \leq 1</math> mA/ch (max)</b>																
<b>OPAy334</b>	Zero Drift, Precision, CMOS Shutdown	1, 2	2.7	5.5	0.35	2	1.6	0.005	0.02	200	110	—	Y	Out	MSOP, SOIC, SOT23	0.95
<b>OPAy335</b>	Zero Drift, Precision, CMOS	1, 2	2.7	5.5	0.35	2	1.6	0.005	0.02	200	110	—	Y	Out	MSOP, SOIC, SOT23	0.95
OPAy277	High Precision, Low Power	1, 2, 4	4	36	0.825	1	0.8	0.02	0.1	1000	130	8	N	N	PDIP, SOIC	0.92
OPAy234	Low Power, Precision	1, 2, 4	2.7	36	0.3	0.35	0.2	0.1	0.5	-25000	96	25	Y	N	MSOP, SOIC	0.99
OPA237	Low Power, Bipolar	1, 2	2.7	36	0.35	1.5	0.5	0.75	2	-40000	78	28	Y	N	SOT23, SOIC	0.49
OPAy336	CMOS, $\mu$ Power	1, 2, 4	2.3	5.5	0.032	0.1	0.03	0.125	1.5	10	80	40	Y	Out	MSOP, PDIP, SOIC, SOT23	0.61
OPAy340	CMOS, Wide Bandwidth	1, 2, 4	2.7	5.5	0.95	5.5	6	0.5	2.5	10	80	25	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy241	Bipolar, $\mu$ Power, High CMRR	1, 2, 4	2.7	36	0.025	0.35	0.1	0.25	0.4	2000	124	45	Y	Out	PDIP, SOIC	1.07
OPAy251	Bipolar, $\mu$ Power, High CMRR, Low Offset Voltage	1, 2, 4	2.7	36	0.025	0.35	0.1	0.25	0.4	2000	124	45	Y	Out	PDIP, SOIC	1.07
TLC1078	Low Voltage, Precision	2	1.4	16	0.017	0.085	0.032	0.45	1.1	70	600	68	N	—	SOIC, SOP, PDIP	2.17
<b>OPAy363</b>	1.8 V, High CMRR, Shutdown	1, 2	1.8	5.5	0.75	7	5	0.5	2	10	74	17	Y	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR	1, 2, 4	1.8	5.5	0.75	7	5	0.5	2	10	74	17	Y	I/O	MSOP, SOIC, SOT23, TSSOP	0.55

<sup>1</sup>New products appear in **BOLD RED**. x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Precision Operational Amplifiers ( $V_{OS} \leq 500 \mu V$ ) Selection Guide (Continued)

Device <sup>1</sup>	Description	Ch.	$V_S$ (V) (min)	$V_S$ (V) (max)	$I_Q$ Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	$V_{OS}$ (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	$I_B$ (pA) (max)	CMRR (dB) (min)	$V_N$ at 1 kHz (nV/ $\sqrt{Hz}$ ) (typ)	Single Supply	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Precision, Low Input Bias Current <math>I_B \leq 100 \text{ pA}</math> (max)</b>																
OPAy132	Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	4.8	8	20	0.5	2	50	96	8	N	N	PDIP, SOIC	1.35
OPA627	Ultra-Low THD+N, DiFET	1	9	36	7.5	16	55	0.1	0.4	5	106	5.2	N	N	PDIP, SOIC, TO-99	9.63
OPA637	Decompensated OPA627	1	9	36	7.5	80	135	0.1	0.4	5	106	4.5	N	N	PDIP, SOIC, TO-99	9.63
OPAy340	CMOS, Wide Bandwidth	1, 2, 4	2.7	5.5	0.95	5.5	6	0.5	2.5	10	80	25	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy350	CMOS, 38 MHz	1, 2, 4	2.7	5.5	7.5	38	22	0.5	4	10	76	5	Y	I/O	PDIP, MSOP, SOIC, SSOP	1.23
<b>OPAy334</b>	Zero-Drift, Precision, CMOS, Shutdown	1, 2	2.7	5.5	0.35	2	1.6	0.005	0.02	200	110	—	Y	Out	MSOP, SOIC, SOT23	0.95
<b>OPAy335</b>	Zero-Drift, Precision, CMOS	1, 2	2.7	5.5	0.35	2	1.6	0.005	0.02	200	110	—	Y	Out	MSOP, SOIC, SOT23	0.95
OPAy336	CMOS, $\mu$ Power	1, 2, 4	2.3	5.5	0.032	0.1	0.03	0.125	1.5	10	80	40	Y	Out	MSOP, PDIP, SOIC, SOT23	0.61
TLC1078	Low Voltage, Precision	2	1.4	16	0.017	0.085	0.032	0.45	1.1	70	600	68	N	—	SOIC, SOP, PDIP	2.17
TLC220x	Precision, Low Noise	1, 2	4.6	16	1.5	1.8	2.5	0.5	0.5	100	85	8	Y	Out	PDIP, SOIC	1.55
<b>Precision, Wide Bandwidth <math>GBW \geq 5 \text{ MHz}</math> (typ)</b>																
<b>OPAy363</b>	1.8 V, High CMRR, SHDN	1, 2	1.8	5.5	0.75	7	5	0.5	2	10	74	17	Y	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR	1, 2, 4	1.8	5.5	0.75	7	5	0.5	2	10	74	17	Y	I/O	MSOP, SOIC, SOT23, TSSOP	0.55
OPAy227	Precision, Ultra-Low Noise	1, 2, 4	5	36	3.8	8	2.3	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
OPAy228	Precision, Low Noise, $G \geq 5$	1, 2, 4	5	36	3.8	33	10	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
TLE2027	Precision, Low Noise, Wide Bandwidth, Wide $V_S$	1	8	38	5.3	13	2.8	0.1	0.4	90000	100	2.5	N	N	SOIC	0.83
OPA627	Ultra-Low THD+N, Wide Bandwidth, Precision	1	9	36	7.5	16	55	0.1	0.4	5	106	5.2	N	N	PDIP, SOIC, TO-99	9.63
OPA637	Ultra-Low THD+N, Wide Bandwidth, Precision	1	9	36	7.5	80	135	0.1	0.4	1	106	5.2	N	N	PDIP, SOIC, TO-99	9.63
OPAy340	CMOS, Wide Bandwidth	1, 2, 4	2.7	5.5	0.95	5.5	6	0.5	2.5	10	80	25	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy132	Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	4.8	8	20	0.5	2	50	96	8	N	N	PDIP, SOIC	1.35
OPAy350	CMOS, 38 MHz	1, 2, 4	2.7	5.5	7.5	38	22	0.5	4	10	76	5	Y	I/O	PDIP, MSOP, SOIC, SSOP	1.23

<sup>1</sup>New products appear in **BOLD RED**. x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Low-Voltage Operational Amplifiers ( $V_S \leq 2.7 \text{ V}$ ) Selection Guide

Device <sup>1</sup>	Description	Ch.	SHDN	$V_S$ (V) (min)	$V_S$ (V) (max)	$I_Q$ Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	$V_{OS}$ (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	$I_B$ (pA) (max)	$V_N$ at 1 kHz (nV/ $\sqrt{Hz}$ ) (typ)	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Low-Voltage, Low Input Bias Current <math>I_B \leq 100 \text{ pA}</math> (max)</b>															
<b>OPAy349</b>	1 $\mu$ A, CMOS, SS	1, 2	N	1.8	5.5	0.002	0.07	0.02	10	10	10	300	I/O	<b>SC70</b> , SOIC, SOT23, SOT23-8(D)	0.70
<b>OPAy363</b>	1.8 V, High CMRR, SS	1, 2	Y	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR, SS	1, 2, 4	N	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23, TSSOP	0.55

<sup>1</sup>New products appear in **BOLD RED**. x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Low-Voltage Operational Amplifiers ( $V_S \leq 2.7\text{ V}$ ) Selection Guide (Continued)

Device <sup>1</sup>	Description	Ch.	SHDN	$V_S$ (V) (min)	$V_S$ (V) (max)	$I_Q$ Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	$V_{OS}$ (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	$I_B$ (pA) (max)	$V_N$ at 1 kHz (nV/ $\sqrt{\text{Hz}}$ ) (typ)	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Low-Voltage, Low Input Bias Current <math>I_B \leq 100\text{ pA}</math> (max)</b>															
TLV276x	1.8 V, $\mu$ Power, SS, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.028	0.5	0.2	3.5	9	15	95	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.61
TLV278x	1.8 V, Low Power, SS, 8 MHz, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.82	8	4.3	3	8	15	18	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.65
<b>OPAy348</b>	High Open-Loop Gain, CMOS, SS	1, 2, 4	N	2.1	5.5	0.065	1	0.5	5	2	10	35	I/O	SC70, SOIC, SOT23, SOT23-8(D), TSSOP	0.50
OPAy336	CMOS, $\mu$ Power, SS	1, 2, 4	N	2.3	5.5	0.032	0.1	0.03	0.125	1.5	10	40	Out	MSOP, PDIP, SOIC, SOT23	0.61
OPAy347	$\mu$ Power, Low Cost, CMOS, SS	1, 2, 4	N	2.3	5.5	0.034	0.35	0.17	6	2	10	60	I/O	PDIP, SC70, SOIC, SOT23, SOT23-8(D), TSSOP	0.46
TLV277x	RRO, SS, High Slew Rate	1, 2, 4	Y	2.5	5.5	2	4.8	9	2.5	2	100	21	Out	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy340	CMOS, Wide Bandwidth, SS	1, 2, 4	N	2.7	5.5	0.95	5.5	6	0.5	2.5	10	25	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy341	Low Voltage, Wide Bandwidth	1, 2	Y	2.7	5.5	1	5.5	6	6	2	10	25	I/O	MSOP, SOIC, SOT23	0.74
OPAy350	SS, CMOS, 38 MHz	1, 2, 4	N	2.7	5.5	7.5	38	22	0.5	4	10	5	I/O	PDIP, MSOP, SOIC, SSOP	1.23
TLV247x	Low Power, SS, Low Bias Current, 35-mA Drive	1, 2, 4	Y	2.7	6	0.75	2.8	1.4	2.2	0.4	50	15	I/O	MSOP(PP), PDIP, SOIC, SOT23, TSSOP(PP)	0.59
<b>Low-Voltage, Low Power <math>I_Q \leq 1\text{ mA}</math> (max)</b>															
TLC1078	Low Voltage, Precision	2	N	1.4	16	0.017	0.085	0.032	0.45	1.1	600	68	—	SOIC, SOP, PDIP	2.17
TLC1079	Low Voltage, Precision	4	N	1.4	16	0.017	0.085	0.032	0.85	1.1	600	68	—	SOIC, SOP, PDIP	3.03
<b>OPAy349</b>	1 $\mu$ A, CMOS, SS	1, 2	N	1.8	5.5	0.002	0.07	0.02	10	15	10	300	I/O	SC70, SOIC, SOT23, SOT23-8(D)	0.70
TLV276x	1.8 V, $\mu$ Power, SS, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.028	0.5	0.2	3.5	9	15	95	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.61
<b>OPAy363</b>	1.8 V, High CMRR, SS	1, 2	Y	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR, SS	1, 2, 4	N	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23, TSSOP	0.55
TLV278x	1.8 V, Low Power, SS, 8 MHz, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.82	8	4.3	3	8	15	18	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.65
<b>OPAy348</b>	High Open-Loop Gain, CMOS, SS	1, 2, 4	N	2.1	5.5	0.065	1	0.5	5	2	10	35	I/O	SC70, SOIC, SOT23, SOT23-8(D), TSSOP	0.50
OPAy336	CMOS, $\mu$ Power, SS	1, 2, 4	N	2.3	5.5	0.032	0.1	0.03	0.125	1.5	10	40	Out	MSOP, PDIP, SOIC, SOT23	0.61
<b>OPAy347</b>	$\mu$ Power, Low Cost, CMOS, SS	1, 2, 4	N	2.3	5.5	0.034	0.35	0.17	6	2	10	60	I/O	PDIP, SC70, SOIC, SOT23, SOT23-8(D), TSSOP	0.46
TLV240x	2.5 V, sub- $\mu$ Power, SS	1, 2, 4	N	2.5	16	0.00095	0.0055	0.0025	1.2	3	300	800	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.95
TLV224x	Low Voltage, 1 $\mu$ A, SS	1, 2, 4	N	2.5	12	0.0012	0.0055	0.002	3	3	500	800	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.56
TLV245x	$\mu$ Power, SS	1, 2, 4	Y	2.7	6	0.035	0.22	0.12	1.5	0.3	5000	51	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.59
<b>OPAy334</b>	Zero Drift, Precision, CMOS, SS	1, 2	Y	2.7	5.5	0.35	2	1.6	0.005	0.02	200	—	Out	MSOP, SOIC, SOT23	0.95
<b>OPAy335</b>	Zero Drift, Precision, CMOS, SS	1, 2	N	2.7	5.5	0.35	2	1.6	0.005	0.02	200	—	Out	MSOP, SOIC, SOT23	0.95
TLV246x	Low Noise, SS, Wide Bandwidth, 25-mA Drive	1, 2, 4	Y	2.7	6	0.575	5.2	1.6	2	2	14000	11	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.59
TLV247x	Low Power, SS, Low Bias Current, 35-mA Drive	1, 2, 4	Y	2.7	6	0.75	2.8	1.4	2.2	0.4	50	15	I/O	MSOP(PP), PDIP, SOIC, SOT23, TSSOP(PP)	0.59
TLV237x	550 $\mu$ A, 3 MHz, SS	1, 2, 4	Y	2.7	15	0.66	3	2.4	4.5	2	60	39	I/O	SOT23, MSOP	0.45
<b>Low-Voltage, Wide Bandwidth <math>GBW \geq 5\text{ MHz}</math> (typ)</b>															
<b>OPAy363</b>	1.8 V, High CMRR, SS	1, 2	Y	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR, SS	1, 2, 4	N	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23, TSSOP	0.55
TLV278x	1.8 V, Low Power, SS, 8 MHz, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.82	8	4.3	3	8	15	18	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.65

<sup>1</sup>New products appear in **BOLD RED**. x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.



## Low-Voltage Operational Amplifiers ( $V_S \leq 2.7\text{ V}$ ) Selection Guide (Continued)

Device <sup>1</sup>	Description	Ch.	SHDN	$V_S$ (V) (min)	$V_S$ (V) (max)	$I_O$ Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	$V_{OS}$ (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	$I_B$ (pA) (max)	$V_N$ at 1 kHz (nV/ $\sqrt{\text{Hz}}$ ) (typ)	Rail-to-Rail	Package(s)	Price <sup>2</sup>
<b>Low-Voltage, Wide Bandwidth GBW <math>\geq 5\text{ MHz}</math> (typ) (Continued)</b>															
TLV277x	SS, High Slew Rate	1, 2, 4	Y	2.5	5.5	2	4.8	9	2.5	2	100	21	Out	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
<b>OPAy357</b>	High Speed, CMOS, SS	1, 2	Y	2.5	5.5	6	100	150	8	4	50	6.5	I/O	SOT23, SOIC, MSOP	0.69
<b>OPAy354</b>	CMOS, 250 MHz, SS	1, 2, 4	N	2.5	5.5	6	100	150	8	4	50	6.5	I/O	SOT23, SOIC, MSOP, TSSOP, SOIC PowerPAD™	0.69
<b>OPAy355</b>	High Speed, CMOS, SS	1, 2, 3	Y	2.5	5.5	11	200	300	9	7	50	5.8	Out	SOT23, SOIC, MSOP, TSSOP	0.85
<b>OPAy356</b>	CMOS, 200 MHz, SS	1, 2	N	2.5	5.5	11	200	300	9	7	50	5.8	Out	SOT23, SOIC, MSOP	0.85
TLV246x	Low Noise, SS, Wide Bandwidth, 25-mA Drive	1, 2, 4	Y	2.7	6	0.575	5.2	1.6	2	2	14000	11	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.59
OPAy340	CMOS, Wide Bandwidth, SS	1, 2, 4	N	2.7	5.5	0.95	5.5	6	0.5	2.5	10	25	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy341	Low Voltage, Wide Bandwidth, SS	1, 2	Y	2.7	5.5	1	5.5	6	6	2	10	25	I/O	MSOP, SOIC, SOT23	0.74
TLV263x	1 mA/ch, 9 MHz, $V_{IN}$ to GND	1, 2, 4	Y	2.7	5.5	1	9	6	3.5	3	50	50	Out	MSOP, PDIP, SOIC, SOT23, TSSOP	0.71
OPAy350	SS, CMOS, 38 MHz	1, 2, 4	N	2.7	5.5	7.5	38	22	0.5	4	10	5	I/O	PDIP, MSOP, SOIC, SSOP	1.23
OPA353	High Speed, Low Voltage, SS, Low THD+N	1, 2, 4	—	2.7	5.5	8	44	22	8	—	—	—	I/O	SOT23, SOIC, MSOP, TSSOP	1.05

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## Low-Power Operational Amplifiers ( $I_O \leq 1\text{ mA}$ ) Selection Guide

Device <sup>1</sup>	Description	Ch.	SHDN	$V_S$ (V) (min)	$V_S$ (V) (max)	$I_O$ Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	$V_{OS}$ (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	$I_B$ (pA) (max)	$V_N$ at 1 kHz (nV/ $\sqrt{\text{Hz}}$ ) (typ)	Rail-to-Rail	Package(s)	Price <sup>2</sup>
<b>Low-Power, Low Voltage <math>V_S \leq 2.7\text{ V}</math> (min)</b>															
TLV240x	2.5 V, sub- $\mu$ Power, SS	1, 2, 4	N	2.5	16	0.00095	0.0055	0.0025	1.2	3	300	800	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.95
TLV224x	Low Voltage, 1 $\mu$ A, SS	1, 2, 4	N	2.5	12	0.0012	0.0055	0.002	3	3	500	800	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.56
TLC1078	Low Voltage, Precision	2	N	1.4	16	0.017	0.085	0.032	0.45	1.1	600	68	—	SOIC, SOP, PDIP	2.17
<b>OPAy349</b>	1 $\mu$ A, CMOS, SS	1, 2	N	1.8	5.5	0.002	0.07	0.02	10	10	15	300	I/O	<b>SC70</b> , SOIC, SOT23, SOT23-8(D)	0.70
OPAy336	CMOS, $\mu$ Power, SS	1, 2, 4	N	2.3	5.5	0.032	0.1	0.03	0.125	1.5	10	40	Out	MSOP, PDIP, SOIC, SOT23	0.61
<b>OPAy347</b>	$\mu$ Power, Low Cost, CMOS, SS	1, 2, 4	N	2.3	5.5	0.034	0.35	0.17	6	2	10	60	I/O	PDIP, <b>SC70</b> , SOIC, SOT23, SOT23-8(D), TSSOP	0.46
TLV245x	$\mu$ Power, SS	1, 2, 4	Y	2.7	6	0.035	0.22	0.12	1.5	0.3	5000	51	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.59
OPAy251	$\mu$ Power, Precision, Optimized for $\pm 15\text{ V}$	1, 2, 4	N	2.7	36	0.038	0.035	0.01	0.25	0.5	-20000	45	Out	PDIP, SOIC	1.07
OPAy244	$\mu$ Power, SS, Low Cost	1, 2, 4	N	2.6	36	0.05	0.24	0.1	1.5	4	-25000	22	N	MSOP, PDIP, SOIC, SOT23, TSSOP	0.50
<b>OPAy348</b>	High Open-Loop Gain, CMOS, SS	1, 2, 4	N	2.1	5.5	0.065	1	0.5	5	2	10	35	I/O	<b>SC70</b> , SOIC, SOT23, SOT23-8(D), TSSOP	0.50
<b>OPAy334</b>	Zero Drift, Precision, CMOS, SS	1, 2	Y	2.7	5.5	0.35	2	0.5	0.005	0.02	200	—	Out	MSOP, SOIC, SOT23	0.95
<b>OPAy335</b>	Zero Drift, Precision, CMOS, SS	1, 2	N	2.7	5.5	0.35	2	0.5	0.005	0.02	200	—	Out	MSOP, SOIC, SOT23	0.95
TLV246x	Low Noise, SS, Wide Bandwidth, 25-mA Drive	1, 2, 4	Y	2.7	6	0.575	5.2	1.6	2	2	14000	11	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.59
<b>OPAy363</b>	1.8 V, High CMRR, SS	1, 2	Y	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR, SS	1, 2, 4	N	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23, TSSOP	0.55

<sup>1</sup>New products appear in **BOLD RED**. *x* indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. *y* indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Low-Power Operational Amplifiers ( $I_Q \leq 1 \text{ mA}$ ) Selection Guide (Continued)

Device <sup>1</sup>	Description	Ch.	SHDN	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	I <sub>Q</sub> Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/μs) (typ)	V <sub>OS</sub> (25°C) (mV) (max)	Offset Drift (μV/°C) (typ)	I <sub>B</sub> (pA) (max)	V <sub>N</sub> at 1 kHz (nV/√Hz) (typ)	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Low-Power, Low Voltage V<sub>S</sub> ≤ 2.7 V (min) (Continued)</b>															
TLV247x	Low Power, SS, Low Bias Current, 35-mA Drive	1, 2, 4	Y	2.7	6	0.75	2.8	1.4	2.2	0.4	50	15	I/O	MSOP(PP), PDIP, SOIC, SOT23, TSSOP(PP)	0.59
TLV278x	1.8 V, Low Power, SS, 8 MHz, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.82	8	4.3	3	8	15	18	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.65
OPAy340	CMOS, Wide Bandwidth, SS	1, 2, 4	N	2.7	5.5	0.95	5.5	6	0.5	2.5	10	25	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
<b>Low-Power, Wide Bandwidth GBW ≥ 5 MHz (typ)</b>															
TLV246x	Low Noise, SS, Wide Bandwidth, 25-mA Drive	1, 2, 4	Y	2.7	6	0.575	5.2	1.6	2	2	14000	11	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.59
<b>OPAy363</b>	1.8 V, High CMRR, SS	1, 2	Y	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23	0.55
<b>OPAy364</b>	1.8 V, High CMRR, SS	1, 2, 4	N	1.8	5.5	0.75	7	5	0.5	2	10	17	I/O	MSOP, SOIC, SOT23, TSSOP	0.55
TLV278x	1.8 V, Low Power, SS, 8 MHz, Low Bias Current	1, 2, 4	Y	1.8	3.6	0.82	8	4.3	3	8	15	18	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.65
OPAy340	CMOS, Wide Bandwidth, SS	1, 2, 4	N	2.7	5.5	0.95	5.5	6	0.5	2.5	10	25	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.67
OPAy341	Low Voltage, Wide Bandwidth, SS	1, 2	Y	2.7	5.5	1	5.5	6	6	2	10	25	I/O	MSOP, SOIC, SOT23	0.74
TLV263x	1 mA/ch, 9 MHz, V <sub>IN</sub> to GND, SS	1, 2, 4	Y	2.7	5.5	1	9	6	3.5	3	50	50	Out	MSOP, PDIP, SOIC, SOT23, TSSOP	0.71

<sup>1</sup>New products appear in **BOLD RED**. x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Wide-Voltage Range Operational Amplifiers ( $\pm 5 \text{ V} \leq V_S \leq \pm 20 \text{ V}$ ) Selection Guide

Device <sup>1</sup>	Description	Ch.	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	I <sub>Q</sub> Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/μs) (typ)	V <sub>OS</sub> (25°C) (mV) (max)	Offset Drift (μV/°C) (typ)	I <sub>B</sub> (pA) (max)	CMRR (dB) (min)	V <sub>N</sub> at 1 kHz (nV/√Hz) (typ)	Single Supply	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Wide-Voltage, Precision Offset V<sub>OS</sub> ≤ 500 μV (max)</b>																
TLC220x	Precision, Low Noise	1, 2	4.6	16	1.5	1.8	2.5	0.5	0.5	100	85	8	Y	Out	PDIP, SOIC	1.55
OPAy234	Low Power, Precision	1, 2, 4	2.7	36	0.3	0.35	0.2	0.1	0.5	-25000	96	25	Y	N	MSOP, SOIC	0.99
OPAy241	μPower, Precision, Optimized for +5 V	1, 2, 4	2.7	36	0.03	0.035	0.01	0.25	0.4	-20000	80	45	Y	Out	PDIP, SOIC	1.07
OPAy251	μPower, Precision, Optimized for ±15 V	1, 2, 4	2.7	36	0.038	0.035	0.01	0.25	0.5	-20000	100	45	Y	Out	PDIP, SOIC	1.07
OPAy277	High Precision, Low Power	1, 2, 4	4	36	0.825	1	0.8	0.02	0.1	1000	130	8	N	N	PDIP, SOIC	0.92
OPAy132	Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	4.8	8	20	0.5	2	50	96	8	N	N	PDIP, SOIC	1.35
OPAy227	Precision, Low Noise	1, 2, 4	5	36	3.8	8	2.3	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
OPAy228	Precision, Low Noise, G ≥ 5	1, 2, 4	5	36	3.8	33	10	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
OPA627	Ultra-Low THD+N, Wide Bandwidth, Precision	1	9	36	7.5	16	55	0.1	0.4	1	106	5.2	N	N	PDIP, SOIC, TO-99	9.63
TLE2027	Precision, Low Noise, Wide Bandwidth, Wide V <sub>S</sub>	1	8	38	5.3	13	2.8	0.1	0.4	90000	100	2.5	N	N	SOIC	0.83
<b>Wide-Voltage, Low Power I<sub>Q</sub> ≤ 1 mA/ch (max)</b>																
OPAy703	12 V, CMOS, Low Power	1, 2, 4	4	12	0.2	1	0.6	0.75	4	10	70	45	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	1.21
OPAy704	12 V, CMOS, Low Power, G ≥ 5	1, 2, 4	4	12	0.2	3	3	0.75	4	10	70	45	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	1.21
OPAy705	12 V, CMOS, Low Power, Low Cost	1, 2, 4	4	12	0.2	1	0.6	5		10	66	45	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	1.02
TLV237x	550 μA, 3 MHz, SHDN	1, 2, 4	2.7	15	0.66	3	2.4	4.5	2	60	57	39	Y	I/O	SOT23, MSOP	0.45

<sup>1</sup>x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Wide-Voltage Range Operational Amplifiers ( $\pm 5\text{ V} \leq V_S \leq \pm 20\text{ V}$ ) Selection Guide (Continued)

Device <sup>1</sup>	Description	Ch.	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	I <sub>Q</sub> Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	V <sub>OS</sub> (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	I <sub>B</sub> (pA) (max)	CMRR (dB) (min)	V <sub>N</sub> at 1 kHz (nV/ $\sqrt{\text{Hz}}$ ) (typ)	Single Supply	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Wide-Voltage, Low Power I<sub>Q</sub> ≤ 1 mA/ch (max) (Continued)</b>																
TLV240x	2.5 V, sub- $\mu$ Power	1, 2, 4	2.5	16	0.00095	0.0055	0.0025	1.2	3	300	63	800	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.95
OPAy241	$\mu$ Power, Precision, Optimized for +5 V	1, 2, 4	2.7	36	0.03	0.035	0.01	0.25	0.4	-20000	80	45	Y	Out	PDIP, SOIC	1.07
OPAy251	$\mu$ Power, Precision, Optimized for +15 V	1, 2, 4	2.7	36	0.038	0.035	0.01	0.25	0.5	-20000	100	45	Y	Out	PDIP, SOIC	1.07
OPAy244	$\mu$ Power, Low Cost	1, 2, 4	2.6	36	0.05	0.24	0.1	1.5	4	-25000	84	22	Y	N	MSOP, PDIP, SOIC, SOT23, TSSOP	0.50
OPAy137	Low Cost, FET-Input, Input to V+	1, 2, 4	4.5	36	0.27	1	3.5	3	15	100	76	45	Y	N	PDIP, SOIC, SOT23, MSOP	0.56
OPAy234	Low Power, Precision	1, 2, 4	2.7	36	0.3	0.35	0.2	0.1	0.5	-25000	96	25	Y	N	MSOP, SOIC	0.99
OPAy237	Low Cost, Low Power	1, 2	2.7	36	0.35	1.4	0.5	0.75	2	-40000	78	28	Y	N	MSOP, SOIC, SOT23	0.51
TLE206x	Low Power, JFET-Input, High Drive	1, 2, 4	7	36	0.35	2	3.4	3	6	2000	65	40	N	N	PDIP, SOIC, TSSOP	0.63
OPAy130	Low Power, FET-Input	1, 2, 4	4.5	36	0.65	1	2	1	2	20	90	16	N	N	SOIC	1.32
OPAy277	High Precision, Low Power	1, 2, 4	4	36	0.825	1	0.8	0.02	0.1	1000	130	8	N	N	PDIP, SOIC	0.92
TLE202x	Low Power, Wide Voltage Supply	1, 2, 4	4	40	0.3	1.2	0.5	0.6	2	70000	85	17	Y	N	PDIP, SOIC, SSOP, TSSOP	0.42
<b>Wide-Voltage, Low Input Bias Current I<sub>B</sub> ≤ 100 pA (max)</b>																
OPAy703	12 V, CMOS, Low Power	1, 2, 4	4	12	0.2	1	0.6	0.75	4	10	70	45	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	1.21
OPAy704	12 V, CMOS, Low Power, G ≥ 5	1, 2, 4	4	12	0.2	3	3	0.75	4	10	70	45	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	1.21
OPAy705	12 V, CMOS, Low Power, Low Cost	1, 2, 4	4	12	0.2	1	0.6	5	—	10	66	45	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	1.02
OPAy743	12 V, 7 MHz, CMOS G ≥ 5	1, 2, 4	3.5	12	1.5	7	10	7	8	10	66	30	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.88
TLV237x	550 $\mu$ A, 3 MHz, SHDN	1, 2, 4	2.7	15	0.66	3	2.4	4.5	2	60	57	39	Y	I/O	SOT23, MSOP	0.45
TLC07x	Low Noise, Wide Bandwidth, CMOS, SHDN, High Drive, Input to V+	1, 2, 4	4.5	16	2.5	10	16	1	1.2	50	100	7	Y	N	MSOP(PP), PDIP, SOIC, TSSOP(PP)	0.46
TLC08x	Low Noise, Wide Bandwidth, CMOS, Input to V-, SHDN, High Drive	1, 2, 4	4.5	16	2.5	10	16	1	1.2	50	100	8.5	Y	N	MSOP(PP), PDIP, SOIC, TSSOP(PP)	0.46
TLC220x	Precision, Low Noise	1, 2	4.6	16	1.5	1.8	2.5	0.5	0.5	100	85	8	Y	Out	PDIP, SOIC	1.55
OPAy130	Low Power, FET-Input	1, 2, 4	4.5	36	0.65	1	2	1	2	20	90	16	N	N	SOIC	1.32
OPAy132	Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	4.8	8	20	0.5	2	50	96	8	N	N	PDIP, SOIC	1.35
OPAy134	Audio, Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	5	8	20	2	2	100	86	8	N	N	PDIP, SOIC	0.88
OPA627	Ultra-Low THD+N, Wide Bandwidth, Precision	1	9	36	7.5	16	55	0.1	0.4	1	106	5.2	N	N	PDIP, SOIC, TO-99	9.63
<b>Wide-Voltage, Wide Bandwidth GBW ≥ 5 MHz (typ)</b>																
OPAy743	12 V, 7 MHz, CMOS, G ≥ 5	1, 2, 4	3.5	12	1.5	7	10	7	8	10	66	30	Y	I/O	MSOP, PDIP, SOIC, SOT23, TSSOP	0.88
TLC07x	Low Noise, Wide Bandwidth, CMOS, SHDN, High Drive, Input to V+	1, 2, 4	4.5	16	2.5	10	16	1	1.2	50	100	7	Y	N	MSOP(PP), PDIP, SOIC, TSSOP(PP)	0.46

<sup>1</sup>x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Wide-Voltage Range Operational Amplifiers ( $\pm 5\text{ V} \leq V_S \leq \pm 20\text{ V}$ ) Selection Guide (Continued)


Device <sup>1</sup>	Description	Ch.	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	I <sub>Q</sub> Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	V <sub>OS</sub> (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	I <sub>B</sub> (pA) (max)	CMRR (dB) (min)	V <sub>N</sub> at 1 kHz (nV/ $\sqrt{\text{Hz}}$ ) (typ)	Single Supply	Rail- to- Rail	Package(s)	Price <sup>2</sup>
<b>Wide-Voltage, Wide Bandwidth GBW <math>\geq 5\text{ MHz}</math> (typ) (Continued)</b>																
TLC08x	Low Noise, Wide Bandwidth, CMOS, Input to V <sub>-</sub> , SHDN, High Drive	1, 2, 4	4.5	16	2.5	10	16	1	1.2	50	100	8.5	Y	N	MSOP(PP), PDIP, SOIC, TSSOP(PP)	0.46
OPAy132	Wide Bandwidth, FET-Input	1, 2, 4	4.5	36	4.8	8	20	0.5	2	50	96	8	N	N	PDIP, SOIC	1.35
OPAy227	Precision, Ultra-Low Noise	1, 2, 4	5	36	3.8	8	2.3	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
OPAy228	Precision, Ultra-Low Noise, G $\geq 5$	1, 2, 4	5	36	3.8	33	10	0.075	0.1	10000	120	3	N	N	PDIP, SOIC	1.01
OPA627	Ultra-Low THD+N, Wide Bandwidth, Precision	1	9	36	7.5	16	55	0.1	0.4	1	106	5.2	N	N	PDIP, SOIC, TO-99	9.63

<sup>1</sup>x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## General Purpose Operational Amplifiers Selection Guide

Device	Description	Ch.	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	I <sub>Q</sub> Per Ch. (mA) (max)	GBW (MHz) (typ)	Slew Rate (V/ $\mu$ s) (typ)	V <sub>OS</sub> (25°C) (mV) (max)	Offset Drift ( $\mu$ V/°C) (typ)	I <sub>B</sub> (pA) (max)	CMRR (dB) (min)	V <sub>N</sub> at 1 kHz (nV/ $\sqrt{\text{Hz}}$ ) (typ)	Single Supply	Package(s)	Price <sup>1</sup>
LF353	JFET-Input	2	7	36	3.25	3	13	10	10	0.2	70	18	N	PDIP, SOIC	0.24
LM358, LM324	Dual, Quad, General Purpose	2, 4	3	32	0.6, 0.3	0.7, 1.2	0.3, 0.5	7	7, —	-250	65	40, 35	Y	PDIP, SOIC, SOP, TSSOP	0.18
LM358A, LM324A	General Purpose	2, 4	3	32	0.6, 0.3	0.7, 1.2	0.3, 0.5	3	7, —	-250	65	40, 35	Y	PDIP, SOIC, SOP, TSSOP	0.27
LM2904, LM2902	General Purpose	2, 4	3	26	0.6, 0.3	0.7, 1.2	0.3, 0.5	7	7, —	-250	50	40, 35	Y	PDIP, SOIC, SOP, TSSOP	0.22
LMV321, LMV358, LMV324	Low Voltage, RRO	1, 2, 4	2.7	5.5	0.17	1	1	7	5	250	50	39	Y	SOT23, SC70, MSOP, SOIC, TSSOP	0.32
LMV324S	Low Voltage, RRO, SHDN	4	2.7	5.5	0.17	1	1	7	5	250	50	39	Y	SOIC, TSSOP	0.35
LT1013/A/D	Precision, Low Power	2	4	44	0.55, 0.5, 0.55	1	0.4	0.3, 0.15, 0.8	2.5, 2, 5	-30, -20, -30	97, 100, 97	22	Y	PDIP, SOIC, CDOP, LCCC	1.12
LT1014/A/D	Precision, Low Power	4	4	44	0.55, 0.5, 0.55	1	0.4	0.3, 0.18, 0.8	2.5, 2, 5	-30, -20, -30	97, 100, 97	22	Y	PDIP, Wide SOIC, CDIP, LCCC	2.94
MC1458	General-Purpose	2	10	30	2.8	1	0.5	6	—	500	70	45	N	PDIP, SOIC, SOP	0.28
MC3403	Low Power, General Purpose	4	5	30	1.75	1	0.6	10	10	-500	70	—	Y	PDIP, SOIC, SOP, TSSOP	0.22
NE5534/A, NE5532/ A	Low Noise	1, 2	10	30	8	10	13, 9	4	—	800	70	4, 5	N	PDIP, SOIC, SOP	0.53
OP07C/D	Precision, Low Offset	1	6	36	5	0.6	0.3	0.15	0.5, 0.7	7, 12	100, 94	9.8	N	PDIP, SOIC, SOP	0.59
RC4558	General Purpose	2	10	30	2.8	3	1.7	6	—	500	70	8	N	PDIP, SOIC, SOP, TSSOP	0.28
TL06x/A/B	Low Power, JFET-Input	1, 2, 4	7	36	0.25	1	3.5	15, 6, 3	10	0.4, 0.2, 0.2	70, 80, 80	42	N	PDIP, SOIC, SOP, TSSOP, CDIP, CFP, LCCC	0.29
TL07x/A/B	Low Noise, JFET-Input	1, 2, 4	7	36	2.5	3	13	10, 6, 3	18	0.2	70, 75, 75	18	N	PDIP, SOIC, SOP, TSSOP, CDIP, CFP, LCCC	0.28
TL08x/A/B	JFET-Input	1, 2, 4	7	36	2.8	3	13	15, 6, 3	18	0.4, 0.2, 0.2	70, 75, 75	18	N	PDIP, SOIC, SOP, TSSOP, CDIP, LCCC	0.29
TL347x	High Slew Rate	2, 4	4	36	4.5	4	13	10	10	500	65	49	Y	PDIP, SOIC	0.49
TLV236x	High Performance, Low Voltage, RRO	1, 2	2	5	2.5	7	3	6	—	150	85	8	N	PDIP, SOT23, SOIC, SOP, TSSOP	0.41
UA741, UA747	General Purpose	1, 2	7	36	2.8	1	0.5	6	—	500	70	—	N	PDIP, SOIC, SOP	0.28

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

 Texas Instruments develops high-speed amps using state-of-the-art processes that generate leading edge performance. Used in next-generation, high-speed signal chains and analog-to-digital drive circuits, high-speed amps are loosely defined as any amplifier having at least 50-MHz of bandwidth and at least 100-V/ $\mu$ s slew rate. High speed amps from TI come in several different types and supply voltage options.

## Design Considerations

**Voltage feedback type**—the most commonly used amp and the basic building block of most analog signal chains such as gain blocks, filtering, level shifting, buffering, etc. Most voltage-feedback amps are unity-gain stable, though some are decompensated to provide wider bandwidth, faster slew rate and lower noise.

**Current feedback type**—most commonly seen in video or xDSL line driver applications, or sockets where extremely fast slew rate is needed. Current-feedback amps are not ideal for filtering applications, as a capacitor in the feedback path can result in unstable operation.

**Fully differential**—the fully differential input and output topology has the primary benefit of reducing even order harmonics, thereby reducing total harmonic distortion. This rejects common-mode components in the signal and provides a larger output swing to the load relative to single-ended amplifiers. Fully differential amplifiers are well-suited to driving analog-to-digital converters. A  $V_{COM}$  pin sets the output common-mode voltage required by most data converters.

**FET-input amplifiers**—have higher input impedance than typical bipolar amps and are more conducive to interfacing to high impedance sources, such as photodiodes in transimpedance circuits.

**Video amplifiers**—can be used in a number of different ways, but generally are in the signal path for amplifying, buffering, filtering or driving video out lines. Typically, the specifications of interest are differential gain and differential phase. Current-feedback amps are typically used in video applications, because of their combination of high slew rate and excellent output drive.

**Fixed and variable gain**—amps are also available with either a fixed gain, or a gain that can be varied either digitally with a few control pins, or linearly with a control voltage. Fixed gain amplifiers are fixed internally with gain setting resistors, usually expecting a specified load. Variable gain amplifiers can have different gain ranges, and can also be fully differential.

**Packaging**—high-speed amplifiers typically come in surface-mount packages, because parasitics of DIP packages can limit performance. Industry standard surface-mount packages (SOIC, MSOP, TSSOP and SOT23) handle the highest-speed bandwidth. For bandwidths approaching 1 GHz and higher, the leadless MSOP package decreases inductance and capacitance.

**Evaluation boards**—all high-speed amps have an associated Evaluation Module (EVM). EVMs are a very important part of high-speed amplifier evaluation, as layout is a critical to design success. To make layout simple, Gerber files of these boards are available. See page 37 for more information.

## High-Speed Amplifiers Selection Tree

Voltage Feedback			Current Feedback
<b>High Speed &lt; 500 MHz</b> — THS4001 — THS4011/4012 — THS4051/4052 — THS4061/4062 — THS4081/4082 — THS4041/4042	<b>FET or CMOS Input</b> — OPA655 — OPA656 — OPA657 (G > 7) — THS4601 — OPA355/2355/3355 — OPA356/2356 — OPA354/2354/4354 — OPA357/2357	<b>Low Noise &lt; 3 nV/<math>\sqrt{\text{Hz}}</math></b> — THS4021/4022 (G $\geq$ 10) — THS4031/4032 (G $\geq$ 2) — OPA642 — OPA686 (G $\geq$ 7) — OPA2822 — THS4130/4131 — THS4271	<b>General Purpose</b> +5 V to $\pm$ 5 V Operational — OPA658/2658 — OPA683/2683 — OPA684/2684/3684/4684* — OPA691/2691/3691 — OPA692/3692 (G = 2 or $\pm$ 1) — OPA2677 — THS3201/02*
<b>Fully Differential</b> — THS4120/4121 — THS4130/4131 — THS4140/4141 — THS4150/4151 — THS4500/4501 — THS4502/4503 — THS4504/4505	<b>Low Voltage <math>\leq</math> 3.3 V</b> — THS4120/21 — OPA355/2355/3355 — OPA356/2356 — THS4222/4226 — OPA354/2354/4354 — OPA357/2357	<b>Variable Gain</b> — THS7001/02 — THS7530* — VCA2612/2613/2614/2616/2618 — VCA610	<b>General Purpose</b> $\pm$ 5 V to $\pm$ 15 V Operational — THS3001 — THS3112/15 — THS3122/25 — THS3061/3062
<b>Very High Speed &gt; 500 MHz</b> — OPA650 — OPA2652 — THS4271 — OPA690/2690/3690 — THS4302 — THS4211/4215	<b>Rail-to-Rail Input or Output</b> — OPA355/2355/3355 — OPA356/2356 — THS4222/4226 — OPA354/2354/4354 — OPA357/2357	<b>Voltage Limiting Output</b> — OPA698* — OPA699* (G $\geq$ 4)	<b>Very High Speed &gt; 500 MHz</b> — OPA658 — OPA695* — THS3201/3202*

\*Preview devices appear in BLUE.



Device <sup>1</sup>	Ch.	SHDN	Supply Voltage (V)	A <sub>CL</sub> (min)	BW at A <sub>CL</sub> (MHz) (typ)	BW G = +2 (MHz) (typ)	GBW Product (MHz) (typ)	Slew Rate (V/μs)	Settling Time 0.1% (ns) (typ)	Distortion			Differential		V <sub>N</sub> (nV/√Hz) (typ)	V <sub>OS</sub> (mV) (max)	I <sub>B</sub> (μA) (max)	I <sub>O</sub> per Ch. (mA) (typ)	I <sub>OUT</sub> (mA) (typ)	Package(s)	Price <sup>2</sup>
										THD 2 V <sub>pp</sub> G = 1 1 MHz (dB) (typ)	1 V <sub>pp</sub> , G = 2, 5 MHz		Gain (%)	Phase (°)							
										HD2 (dBc) (typ)	HD3 (dBc) (typ)										
<b>Fully Differential</b>																					
THS4120/21	1	Y	3	1	100	—	—	55	60	-75	-70	-60	—	—	5.4	8	1.2 pA	11	100	SOIC, MSOP PowerPAD™	1.88
THS4130/31	1	Y	5, ±5, ±15	1	150	90	90	52	78	-97	-60	-75	—	—	1.3	2	6	12.3	85	SOIC, MSOP PowerPAD	3.35
THS4140/41	1	Y	5, ±5, ±15	1	160	—	—	450	96	-79	-65	-55.5	—	—	6.5	7	15	15	85	SOIC, MSOP PowerPAD	3.25
THS4150/51	1	Y	5, ±5, ±15	1	150	81	100	650	53	-84	-72	-73	—	—	7.6	7	15	17.5	85	SOIC, MSOP PowerPAD	4.50
<b>THS4500/01</b>	1	Y	5, ±5	1	370	175	300	2800	6.3	-100	-82	-97	—	—	7	7	4.6	23	120	SOIC, MSOP PowerPAD, Leadless MSOP PowerPAD	3.45
<b>THS4502/03</b>	1	Y	5, ±5	1	370	175	300	2800	6.3	-100	-83	-97	—	—	6	7	15	23	98	SOIC, MSOP PowerPAD, Leadless MSOP PowerPAD	3.77
<b>THS4504/05</b>	1	Y	5, ±5	1	260	110	210	1800	20	-100	-79	-93	—	—	8	7	4.6	100	130	SOIC, MSOP PowerPAD, Leadless MSOP PowerPAD	1.65
<b>Fixed and Variable Gain</b>																					
BUF634	1	—	5, ±5, ±15	1	180	—	—	2000	200	—	—	—	0.4	0.1	4	100	20	15	250	SOIC	2.84
<b>OPA692</b>	1	Y	5, ±5	—	280	225	—	2000	8	-70	-69	-76	0.07	0.02	1.7	2.5	35	5.1	190	SOT23, SOIC	1.35
<b>OPA3692</b>	3	Y	5, ±5	—	280	225	—	2000	8	-74	-69	-76	0.07	0.02	1.7	2.5	35	5.1	190	MSOP, SOIC	2.98
<b>THS4302</b>	1	Y	3, 5	5	2400	—	12000	5500	—	-90	-75	-85	—	—	2.8	4.25	10	37	180	Leadless MSOP PowerPAD	1.97
THS7001	1	Y	±5, ±15	1	—	100	—	85	85	-60	-65	-65	0.02	0.01	1.7	5	6	7	50	TSSOP PowerPAD	5.92
THS7002	2	Y	±5, ±15	1	—	100	—	85	85	-88	-65	-65	0.02	0.01	1.7	5	6	7	50	TSSOP PowerPAD	5.92
<b>THS7530</b>	1	Y	5	—	300	—	—	1750	—	-51	-54	-50	—	—	1.27	—	30	35	20	TSSOP PowerPAD	3.65
<b>CMOS Amplifiers</b>																					
<b>OPA354</b>	1	—	2.5 to 5.5	1	250	90	100	150	30	—	-75	-83	0.02	0.09	6.5	8	50 pA	4.9	100	SOT23, SOIC PowerPAD	0.69
<b>OPA2354</b>	2	—	2.5 to 5.5	1	250	90	100	150	30	—	-75	-83	0.02	0.09	6.5	8	50 pA	4.9	100	SOIC PowerPAD, MSOP	1.14
<b>OPA4354</b>	4	—	2.5 to 5.5	1	250	90	100	150	30	—	-75	-83	0.02	0.09	6.5	8	50 pA	4.9	100	SOIC, TSSOP	1.71
OPA355	1	Y	2.5 to 5.5	1	450	100	200	300	30	—	-81	-93	0.02	0.05	5.8	9	50 pA	8.3	60	SOT23, SOIC	0.85
OPA2355	2	Y	2.5 to 5.5	1	450	100	200	300	30	—	-81	-93	0.02	0.05	5.8	9	50 pA	8.3	60	MSOP	1.40
OPA3355	3	Y	2.5 to 5.5	1	450	100	200	300	30	—	-81	-93	0.02	0.05	5.8	9	50 pA	8.3	60	SOIC	1.79
OPA356	1	—	2.5 to 5.5	1	450	100	200	300	30	—	-81	-93	0.02	0.05	5.8	9	50 pA	8.3	60	SOT23, SOIC	0.85
OPA2356	2	—	2.5 to 5.5	1	450	100	200	300	30	—	-81	-93	0.02	0.05	5.8	9	50 pA	8.3	60	SOIC, MSOP	1.40
<b>OPA357</b>	1	Y	2.5 to 5.5	1	250	90	100	150	30	—	-75	-83	0.02	0.09	6.5	8	50 pA	4.9	100	SOT23, SOIC PowerPAD	0.69
<b>OPA2357</b>	2	Y	2.5 to 5.5	1	250	90	100	150	30	—	-75	-83	0.02	0.09	6.5	8	50 pA	4.9	100	MSOP	1.14
<b>FET-Input</b>																					
OPA655	1	—	±5	1	400	185	240	290	8	-100	-70	-80	0.01	0.01	6	2	125 pA	25	60	SOIC	9.13
OPA656	1	—	±5	1	500	200	230	290	—	-80	-77	-90	0.02	0.05	7	1.8	20 pA	14	70	SOT23, SOIC	5.85
OPA657	1	—	±5	7	350	300	1600	700	10	-80	-73	-100	—	—	4.8	1.8	20 pA	14	70	SOT23, SOIC	7.29
THS4601	1	—	±5, ±15	1	440	95	180	100	135	-76	-80	-83	0.02	0.08	5.4	4	100 pA	10	80	SOIC	9.95
<b>Voltage Feedback</b>																					
OPA642	1	—	±5	1	400	150	210	380	11.5	-100	-82	-100	0.007	0.008	2.7	1	45	20	60	SOT23, SOIC	3.75
OPA643	1	—	±5	5	200	—	800	1000	16.5	-91	-84	-100	0.005	0.015	2.3	1.5	30	20	60	SOT23, SOIC	3.61
OPA650	1	—	±5	1	560	140	180	240	10.2	-80	-76	-69	0.01	0.03	8.4	2.5	10	5.1	110	SOT23, SOIC	1.95


<sup>1</sup>New products appear in **BOLD RED**. Preview devices appear in **BOLD BLUE**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

Device <sup>1</sup>	Ch.	SHDN	Supply Voltage (V)	A <sub>CL</sub> (min)	BW at A <sub>CL</sub> (MHz)	BW G = +2 (MHz)	GBW Product (MHz)	Slew Rate (V/μs)	Settling Time 0.1% (ns)	Distortion			Differential		V <sub>N</sub> (nV/√Hz) (typ)	V <sub>OS</sub> (mV) (max)	I <sub>B</sub> (μA) (max)	I <sub>Q</sub> per Ch. (mA) (typ)	I <sub>OUT</sub> (mA) (typ)	Package(s)	Price <sup>2</sup>
										THD 2 V <sub>pp</sub> G = 1 1 MHz (dB) (typ)	1 V <sub>pp</sub> , G = 2, 5 MHz		Gain (%)	Phase (°)							
											HD2 (dBc) (typ)	HD3 (dBc) (typ)									
<b>Voltage Feedback (Continued)</b>																					
OPA4650	4	—	±5	1	360	120	160	240	10.3	-80	-76	-69	0.01	0.03	8.4	5.5	20	5.7	110	SOIC	4.82
OPA2652	2	—	±5	1	700	200	200	335	—	-75	-76	-66	0.05	0.03	8	7	15	11	140	SOT23, SOIC	1.19
OPA2822	2	—	5, ±5	1	400	200	240	170	32	-86	-75	-86	0.02	0.03	2	1.2	12	4.8	150	SOIC, MSOP	2.17
OPA686	1	—	±5	7	425	—	1600	600	16	-82	-74	-105	0.02	0.02	1.3	1	17	12.4	80	SOT23, SOIC	2.89
OPA2686	2	—	±5	7	425	—	1600	600	16	-80	-69	-97	0.02	0.02	1.4	1	17	12.4	80	SOIC	4.42
OPA687	1	Y	±5	12	600	—	3800	900	15	-85	-77	-110	—	—	0.95	1	33	18.5	80	SOT23, SOIC	3.37
OPA688	1	—	5, ±5	1	530	260	290	1000	7	-66	-67	-86	—	—	6.3	6	12	15.8	105	SOIC	2.56
OPA689	1	—	5, ±5	4	280	—	720	1600	7	-66	-67	-86	0.02	0.01	4.6	5	12	15.8	105	SOIC	2.84
<b>OPA690</b>	1	Y	5, ±5	1	500	220	300	1800	8	-80	-68	-68	0.06	0.03	5.5	4	8	5.5	190	SOT23, SOIC	1.50
<b>OPA2690</b>	2	Y	5, ±5	1	400	220	300	1800	8	-80	-68	-68	0.06	0.03	5.5	4.5	10	5.5	190	SOIC	2.32
<b>OPA3690</b>	3	Y	5, ±5	1	400	220	300	1800	8	-75	-68	-70	0.06	0.01	4.5	4.5	10	5.5	190	SOIC, TSSOP	3.19
THS4001	1	—	5, ±5, ±15	1	270	—	100	400	40	-72	-65	-62	0.04	0.15	12.5	8	5	7.8	100	SOIC	2.19
THS4011	1	—	±5, ±15	1	290	50	100	310	37	-80	-65	-80	0.006	0.01	7.5	6	6	7.8	110	SOIC, MSOP PowerPAD™	2.29
THS4012	2	—	±5, ±15	1	290	50	100	310	37	-80	-65	-80	0.006	0.01	7.5	6	6	7.8	110	SOIC, MSOP PowerPAD	3.81
THS4021	1	—	±5, ±15	10	350	—	1600	470	40	-68	-55	-83	0.02	0.08	1.5	2	6	7.8	100	SOIC, MSOP PowerPAD	1.67
THS4022	2	—	±5, ±15	10	350	—	1600	470	40	-68	-55	-83	0.02	0.08	1.5	2	6	7.8	100	SOIC, MSOP PowerPAD	2.79
THS4031	1	—	±5, ±15	2	100	100	200	100	60	-72	-77	-67	0.015	0.025	1.6	2	6	8.5	90	SOIC, MSOP PowerPAD	2.23
THS4032	2	—	±5, ±15	2	100	100	200	100	60	-72	-73	-67	0.015	0.025	1.6	2	6	8.5	90	SOIC, MSOP PowerPAD	3.68
THS4041	1	—	±5, ±15	1	165	60	100	400	120	-75	-75	-88	0.01	0.01	14	10	6	8	100	SOIC, MSOP PowerPAD	1.25
THS4042	2	—	±5, ±15	1	165	60	100	400	120	-75	-75	-88	0.01	0.01	14	10	6	8	100	SOIC, MSOP PowerPAD	2.49
THS4051	1	—	±5, ±15	1	70	38	—	240	60	-82	-66	-79	0.01	0.01	14	10	6	8.5	100	SOIC, MSOP PowerPAD	1.20
THS4052	2	—	±5, ±15	1	70	38	—	240	60	-82	-66	-79	0.01	0.01	14	10	6	8.5	100	SOIC, MSOP PowerPAD	1.55
THS4061	1	—	±5, ±15	1	180	—	100	400	40	-72	-58	-75	0.02	0.02	14.5	8	6	7.8	115	SOIC, MSOP PowerPAD	1.52
THS4062	2	—	±5, ±15	1	180	—	100	400	40	-72	-58	-75	0.02	0.02	14.5	8	6	7.8	115	SOIC, MSOP PowerPAD	1.92
THS4081	1	—	±5, ±15	1	175	—	100	230	43	-64	-67	-52	0.01	0.05	10	7	6	3.4	85	SOIC, MSOP PowerPAD	1.79
THS4082	2	—	±5, ±15	1	175	—	100	230	43	-64	-67	-52	0.01	0.05	10	7	6	3.4	85	SOIC, MSOP PowerPAD	2.78
<b>THS4211/15</b>	1	Y	5, ±5, 15	1	1000	325	350	970	22	-95	-98	-110	0.007	0.003	7	12	15	19	220	SOIC, MSOP PowerPAD, Leadless MSOP PowerPAD	1.79
THS4222/26	2	Y	3, 5, ±5, ±15	1	230	100	120	975	25	-100	-79	-92	0.007	0.007	13	10	3	14	100	SOIC, MSOP PowerPAD, TSSOP PowerPAD	1.79
<b>THS4271/75</b>	1	Y	5, ±5, 15	1	1400	390	400	1000	25	-110	-100	-94	0.007	0.004	3	10	15	22	160	SOIC, MSOP PowerPAD, Leadless MSOP PowerPAD	2.69
<b>Current Feedback</b>																					
OPA658	1	—	±5	1	900	680	—	1700	11.5	-70	-71	-62	0.025	0.02	2.7	5.5	30	4.5	80	SOT23, SOIC	1.95
OPA2658	2	—	±5	1	900	680	—	1700	11.5	-70	-71	-62	0.025	0.02	2.7	5.5	30	4.5	80	SOIC	3.12
OPA2681	2	Y	5, ±5	1	280	220	—	2100	8	-72	-79	-88	0.001	0.01	2.5	5	55	6	190	SOIC	1.79
<b>OPA683</b>	1	Y	3, 5, ±5	1	200	150	—	540	—	-75	-63	-67	0.06	0.03	4.4	4.1	4.6	1.9	150	SOT23, SOIC	1.15
<b>OPA2683</b>	2	—	3, 5, ±5	1	200	150	—	540	—	-75	-63	-67	0.06	0.03	4.4	4.1	4.6	1.9	150	SOT23, SOIC	1.76

<sup>1</sup>New products appear in **BOLD RED**. Preview devices appear in **BOLD BLUE**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

Device <sup>1</sup>	Ch.	SHDN	Supply Voltage (V)	A <sub>CL</sub> (min)	BW at A <sub>CL</sub> (MHz)	BW G = +2 (MHz)	GBW Product (MHz)	Slew Rate (V/μs)	Settling Time 0.1% (ns)	Distortion			Differential		V <sub>N</sub> (nV/√Hz) (typ)	V <sub>OS</sub> (mV) (max)	I <sub>B</sub> (μA) (max)	I <sub>Q</sub> per Ch. (mA) (typ)	I <sub>OUT</sub> (mA) (typ)	Package(s)	Price <sup>2</sup>
										THD 2 V <sub>pp</sub> G = 1 1 MHz (dB) (typ)	1 V <sub>pp</sub> , G = 2, 5 MHz		Gain (%)	Phase (°)							
											HD2 (dBc) (typ)	HD3 (dBc) (typ)									
<b>Current Feedback (Continued)</b>																					
<b>OPA684</b>	1	Y	5, ±5	1	210	170	—	820	11	-75	-67	-70	0.04	0.02	3.7	3.5	16	1.7	120	SOT23, SOIC	1.30
<b>OPA2684</b>	2	—	5, ±5	1	210	170	—	820	11	-75	-67	-70	0.04	0.02	3.7	3.5	16	1.7	120	SOT23, SOIC	1.97
<b>OPA3684</b>	3	Y	5, ±5	1	210	170	—	820	11	-75	-67	-70	0.04	0.02	3.7	3.5	16	1.7	120	SOIC, TSSOP	2.59
<b>OPA4684</b>	4	—	5, ±5	1	210	170	—	820	11	-75	-67	-70	0.04	0.02	3.7	3.5	16	1.7	120	SOIC, TSSOP	3.15
OPA685	1	Y	5, ±5	1	1200	900	—	4200	3	-80	-66	-90	0.1	0.01	1.7	3.5	90	12.9	130	SOT23, SOIC	1.82
<b>OPA691</b>	1	Y	5, ±5	1	280	225	—	2100	8	-80	-72	-74	0.07	0.02	1.7	2.5	35	5.1	190	SOT23, SOIC	1.45
<b>OPA2691</b>	2	Y	5, ±5	1	280	225	—	2100	8	-80	-72	-74	0.07	0.02	1.7	2.5	35	5.1	190	SOIC	2.32
<b>OPA3691</b>	3	Y	5, ±5	1	280	225	—	2100	8	-80	-72	-74	0.07	0.02	1.7	2.5	35	5.1	190	SOIC, MSOP	3.15
THS3001	1	—	±5, ±15	1	420	385	—	6500	40	-93	-90	-85	0.01	0.02	1.6	3	10	6.6	120	SOIC, MSOP PowerPAD™	3.37
THS3061	1	—	±5, ±15	1	300	275	—	7000	30	-85	-78	-81	0.02	0.01	2.6	3.5	20	8.3	145	SOIC, SOIC PowerPAD, MSOP PowerPAD	2.95
THS3062	2	—	±5, ±15	1	300	275	—	7000	30	-85	-78	-81	0.02	0.01	2.6	3.5	20	8.3	145	SOIC, SOIC PowerPAD, MSOP PowerPAD, MSOP PowerPAD	4.25
<b>THS3091</b>	1	—	±5, ±15	1	250	235	—	7000	30	—	—	—	0.02	0.01	1.7	3	8	7.5	200	SOIC, SOIC PowerPAD,	—
<b>THS3092</b>	2	—	±5, ±15	1	250	235	—	7000	30	—	—	—	0.02	0.01	1.7	3	8	7.5	200	SOIC, SOIC PowerPAD,	—
THS3112/15	2	Y	±5, ±15	1	110	110	—	1550	63	-78	-77	-80	0.01	0.011	2.2	8	23	4.9	270	SOIC, SOIC PowerPAD, TSSOP PowerPAD	3.03
THS3122/25	2	Y	±5, ±15	1	160	128	—	1550	64	-78	-70	-77	0.01	0.011	2.2	6	23	8.4	440	SOIC, SOIC PowerPAD, TSSOP PowerPAD	3.75
THS3202	2	—	±5, 15	1	1200	1000	—	9000	10	-65	-68	-70	0.02	0.01	6.8	4	35	—	115	SOT23, SOIC, MSOP	2.89
<b>xDSL Drivers and Receivers</b>																					
<b>OPA2677</b>	2	—	5, ±5	1	220	200	—	1800	—	-73	-75	-85	0.03	0.01	2	5.5	30	18	500	SOIC, SOIC PowerPAD	2.29
THS6002	4	—	±5, ±15	1	140	120	—	1000	70	-62	-62	-72	0.05	0.08	—	4	8	4.2	95	SOIC WPowerPAD	5.69
THS6007	4	—	±5, ±15	1	140	120	—	1300	70	-70	-72	-72	0.05	0.08	1.7	5	9	11.5	500	TSSOP	6.88
THS6012	2	—	±5, ±15	1	140	120	—	1300	70	-79	-65	-65	0.05	0.08	1.7	5	9	11.5	500	SOIC WPowerPAD, μ*jr-BGA	4.81
THS6022	2	—	±5, ±15	1	210	200	—	1900	70	-75	-55	-58	0.04	0.06	1.7	5	9	7.2	250	TSSOP	2.87
THS6032	2	Y	±5, ±15	1	65	60	—	1200	120	-58	-70	-58	0.016	0.4	2.4	5	9	4	440	SOIC WPowerPAD, μ*jr-BGA, TQFP PowerPAD	5.09
THS6042/43	2	Y	±5, ±15	1	120	95	—	1000	—	-75	-40	-60	—	—	2.2	16	12	8.2	350	SOIC, SOIC PowerPAD, TSSOP	2.68
THS6052/53	2	Y	±5, ±15	1	120	100	—	850	—	-83	—	—	—	—	2.1	10	10	4.5	175	SOIC, SOIC PowerPAD, TSSOP	2.30
THS6062	2	—	5, ±5, ±15	2	100	100	—	100	60	-72	-55	-62	—	—	1.6	6	6	8.5	90	SOIC, MSOP PowerPAD	2.33
THS6072	2	—	±5, ±15	1	175	—	—	230	43	-79	-55	-60	—	—	10	7	6	3.4	85	SOIC, MSOP PowerPAD	2.36
<b>THS6092/93</b>	2	Y	5, ±5	1	100	—	—	600	—	-72	—	—	—	—	2.1	16	10	6.7	240	SOIC, SOIC PowerPAD	1.91
<b>THS6132</b>	1	—	±5, ±15	1	80	70	—	300	—	-100	-83	-100	—	—	3.5	1	1	6.4	500	Leadless MSOP PowerPAD, TQFP PowerPAD	3.85
<b>THS6182</b>	1	—	±5, ±15	1	100	80	—	450	—	-88	-92	-94	—	—	3.2	20	15	11.5	600	SOIC, TSSOP, Leadless MSOP PowerPAD	3.65

<sup>1</sup>New products appear in **BOLD RED**. Preview devices appear in **BOLD BLUE**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

 Comparator ICs are specialized op amps designed to compare two input voltages and provide a logic state output. They can be considered one-bit analog-to-digital converters.

The TI comparator portfolio consists of a variety of products with various performance characteristics, including: fast (ns) response time, wide input voltage ranges, extremely low quiescent current consumption and op amp and comparator combination ICs.

### Comparator vs. Op Amp

	Comparator	Op Amp
Speed (Response time)	Yes	No
Logic Output	Yes	No
Wide Diff. Input Range	Yes	Yes
Precision	No	Yes

In general, if a fast response time is required, always use a comparator.

### Design Considerations

#### Output topology

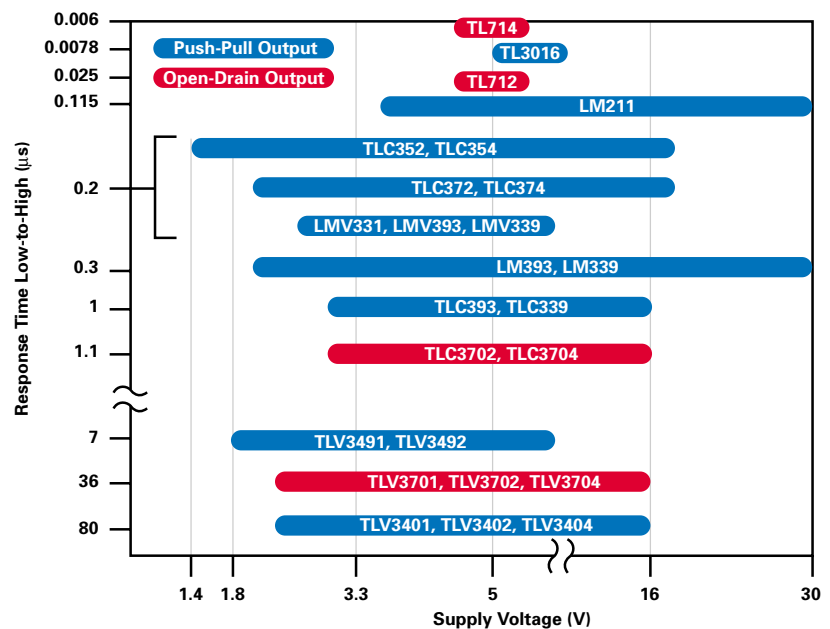
- *Open collector*—connects to the logic supply through a pull-up resistor and allows comparators to interface to a variety of logic families.
- *Push-pull*—does not require a pull-up resistor. Because the output swings rail-to-rail, the logic level is dependent on the voltage supplies of the comparator.

**Response time (propagation delay)**—applications requiring “near real-time” signal response should consider comparators with nanosecond (ns) propagation delay. Note that as propagation delay decreases, supply current increases. Evaluate what mix of performance and power can be afforded. The TLV349x family offers a unique combination of speed/power with 5- $\mu$ s propagation delay on only 1  $\mu$ A of quiescent current.

**Hysteresis**—positive feedback that pulls the input signal through the threshold when the output switches, preventing unwanted multiple switching.

**Combination comparator and op amp**—for input signals requiring DC level shifting and/or gain prior to the comparator, consider the TLV230x (open drain) or TLV270x (push-pull) op amp and comparator combinations. These dual function devices save space and cost!

Comparator Product Portfolio Snapshot



### Comparators Selection Guide

Device <sup>1</sup>	Description	Ch.	I <sub>Q</sub> per Ch. (mA) (max)	Output Current (mA) (min)	t <sub>RESP</sub> Low-to-High (μs)	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	V <sub>OS</sub> (25°C) (mV) (max)	Output Type	Package(s)	Price <sup>2</sup>
<b>High Speed t<sub>RESP</sub> ≤ 0.1 μs</b>											
TL714	Linear	1	12	16	0.006	4.75	5.25	10	Open Drain/Collector	PDIP, SOIC	1.75
TL3016	Comparator	1	12.5	—	0.0078	5	10	3	Open Drain/Collector	SOIC, TSSOP	0.92
TL3116	Ultra Fast, Low Power, Precision	1	14.7	—	0.0099	5	10	3	Open Drain/Collector	SOIC, TSSOP	0.92
TL712	Single, High Speed	1	20	16	0.025	4.75	5.25	5	Open Drain/Collector	PDIP, SOIC, SOP	0.70
LM306	Single, Strobed, General Purpose	1	6.8	100	0.028	-6	12	5	Open Drain/Collector	PDIP, SOIC	0.63
LM211	Single, High Speed, Strobed	1	6	—	0.115	3.5	30	3	Open Drain/Collector	PDIP, SOIC	0.27
LM311	Single, High Speed, Strobed, Diff.	1	7.5	—	0.115	3.5	30	7.5	Open Drain/Collector	PDIP, SOIC, SOP, TSSOP	0.18
LM111	Single, Strobed, Differential	1	6	—	0.165	3.5	30	3	Open Drain/Collector	CDIP, LCCC	1.37
<b>Low Power I<sub>Q</sub> &lt; 0.5 mA</b>											
TLV340x	Nanopower, Open Drain, RRIO	1, 2, 4	0.00055	—	80	2.5	16	3.6	Open Drain/Collector	MSOP, PDIP, SOIC, SOT23, TSSOP	0.56

<sup>1</sup>x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Comparators Selection Guide (Continued)

Device <sup>1</sup>	Description	Ch.	I <sub>Q</sub> per Ch. (mA) (max)	Output Current (mA) (min)	t <sub>RESP</sub> Low-to-High (μs)	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	V <sub>OS</sub> (25°C) (mV) (max)	Output Type	Package(s)	Price <sup>2</sup>
<b>Low Power I<sub>Q</sub> &lt; 0.5 mA (Continued)</b>											
TLV370x	Nanopower, Push-Pull, RRIO	1, 2, 4	0.0008	—	36	2.5	16	5	Push Pull	MSOP, PDIP, SOIC, SOT23, TSSOP	0.56
<b>TLV349x</b>	Low Voltage, Excellent Speed/Power	1, 2, 4	0.0012	—	< 0.1	1.8	5.5	15	Push Pull	SOT23, SOIC, TSSOP	0.55
TLV230x	Sub-Micropower, Op Amp and Comparator, RRIO	2	0.0017	—	55	2.5	16	5	Open Drain/Collector	MSOP, PDIP, SOIC, TSSOP	0.84
TLV270x	Sub-Micropower, Op Amp and Comparator, RRIO	2, 4	0.0019	—	36	2.5	16	5	Push Pull	MSOP, PDIP, SOIC, TSSOP	0.84
TLC370x	Fast, Low Power	2	0.02	4	1.1	3	16	5	Push Pull	PDIP, SOIC, TSSOP	0.35
TLC393	Linear	2	0.02	6	1.1	3	16	5	Open Drain/Collector	PDIP, SOIC, SOP, TSSOP	0.38
TLC339	Quad, Low Power, Open Drain	4	0.02	6	1	3	16	5	Open Drain/Collector	PDIP, SOIC, TSSOP	0.44
LP2901	Quad, Low Power, General Purpose	4	0.025	—	1.3	5	30	5	Open Drain/Collector	PDIP, SOIC	0.56
LP339	Quad, Low Power, General Purpose	4	0.025	—	1.3	5	30	5	Open Drain/Collector	PDIP, SOIC	0.49
LMV393	Dual, Low Voltage	2	0.1	10	0.2	2.7	5.5	7	Open Drain/Collector	SOIC, TSSOP	0.34
LMV339	Quad, Low-Voltage	4	0.1	—	0.2	2.7	5.5	7	Open Drain/Collector	SOIC, TSSOP	0.36
LMV331	Single, Low Voltage	1	0.12	10	0.2	2.7	5.5	7	Open Drain/Collector	SC70, SOT23	0.34
TLC37x	Fast, Low Power	2	0.15	6	0.2	2	18	5	Open Drain/Collector	PDIP, SOIC, TSSOP	0.34
TLV1391	Linear	—	0.15	0.6	0.65	2	7	5	—	SOT23	0.41
LM3302	Quad, General Purpose	4	0.2	6	0.3	2	28	20	Open Drain/Collector	PDIP, SOIC	0.46
LP211	Single, Strobed, Low Power	1	0.3	—	1.2	3.5	30	7.5	Open Drain/Collector	SOIC	0.50
LP311	Single, Strobed, Low Power	1	0.3	1.6	1.2	3.5	30	7.5	Open Drain/Collector	PDIP, SOIC, SOP	0.46
<b>Low Voltage V<sub>S</sub> ≤ 2.7 V (min)</b>											
TLC35x	1.4 V	2	0.15	6	0.2	1.4	18	5	Open Drain/Collector	PDIP, SOIC, TSSOP	0.40
<b>TLV349x</b>	Low Voltage, Excellent Speed/Power	1, 2, 4	0.0012	—	< 0.1	1.8	5.5	15	Push Pull	SOT23, SOIC, TSSOP	0.55
TLV1391	Linear Comparator	—	0.15	0.6	0.65	2	7	5	—	SOT23	0.41
TLV235x	Low Voltage	2, 4	0.125	6	0.2	2	8	5	Open Drain/Collector	PDIP, SOIC, TSSOP	0.84
TLC37x	Fast, Low Power	2	0.15	6	0.2	2	18	5	Open Drain/Collector	PDIP, SOIC, TSSOP	0.34
LM3302	Quad, General Purpose	4	0.2	6	0.3	2	28	20	Open Drain/Collector	PDIP, SOIC	0.46
LM2903	Dual, General Purpose	2	0.5	6	0.3	2	30	7	Open Drain/Collector	PDIP, SOIC, SOP, TSSOP	0.22
LM293	Dual, General Purpose	2	0.5	6	0.3	2	30	5	Open Drain/Collector	PDIP, SOIC	0.28
LM293A	Dual, General Purpose	2	0.5	6	0.3	2	30	3	Open Drain/Collector	SOIC	0.36
LM393	Dual, General Purpose	2	0.5	6	0.3	2	30	5	Open Drain/Collector	PDIP, SOIC, SOP, TSSOP	0.18
LM393A	Dual, General Purpose	2	0.5	6	0.3	2	30	3	Open Drain/Collector	PDIP, SOIC, SOP, TSSOP	0.27
LM239	Quad, General Purpose	4	0.5	6	0.3	2	30	5	Open Drain/Collector	PDIP, SOIC	0.28
LM239A	Quad, General Purpose	4	0.5	6	0.3	2	30	2	Open Drain/Collector	SOIC	0.91
LM2901	Quad, General Purpose	4	0.625	6	0.3	2	30	3	Open Drain/Collector	PDIP, SOIC, SOP, TSSOP	0.22
LM339	Quad, General Purpose	4	0.5	6	0.3	2	30	5	Open Drain/Collector	PDIP, SOIC, SOP, SSOP, TSSOP	0.18
LM339A	Quad, General Purpose	4	0.5	6	0.3	2	30	3	Open Drain/Collector	PDIP, SOIC, SOP	0.27
TL331	Single, Differential	1	0.7	6	0.3	2	36	5	Open Drain/Collector	SOT23	0.28
LM139	Quad	4	0.5	6	0.3	2	36	5	Open Drain/Collector	SOIC	0.54
LM139A	Quad	4	0.5	6	0.3	2	36	2	Open Drain/Collector	SOIC	0.94
LM193	Dual	4	0.5	6	0.3	2	36	5	Open Drain/Collector	SOIC	0.30
TLV340x	Nanopower, Open Drain, RRIO	1, 2, 4	0.00055	—	80	2.5	16	3.6	Open Drain/Collector	MSOP, PDIP, SOIC, SOT23, TSSOP	0.56
TLV370x	Nanopower, Push-Pull, RRIO	1, 2, 4	0.0008	—	36	2.5	16	5	Push Pull	MSOP, PDIP, SOIC, SOT23, TSSOP	0.56
LMV331	Single, Low Voltage	1	0.12	10	0.2	2.7	5.5	7	Open Drain/Collector	SC70, SOT23	0.34
LMV393	Dual, Low Voltage	2	0.1	10	0.2	2.7	5.5	7	Open Drain/Collector	SOIC, TSSOP	0.34
LMV339	Quad Low Voltage Comparators	4	0.1	—	0.2	2.7	5.5	7	Open Drain/Collector	SOIC, TSSOP	0.36
<b>Combination Comparators and Op Amps</b>											
<b>TLV230x</b>	Sub-Micropower, Op Amp and Comparator, RRIO	2	0.0017	—	55	2.5	16	5	Open Drain/Collector	MSOP, PDIP, SOIC, TSSOP	0.84
<b>TLV270x</b>	Sub-Micropower, Op Amp and Comparator, RRIO	2, 4	0.0019	—	36	2.5	16	5	Push Pull	MSOP, PDIP, SOIC, TSSOP	0.84

<sup>1</sup>New products appear in **BOLD RED**. x indicates: 0 = single with shutdown, 1 = single, 2 = dual, 3 = dual with shutdown, 4 = quad, 5 = quad with shutdown. y indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

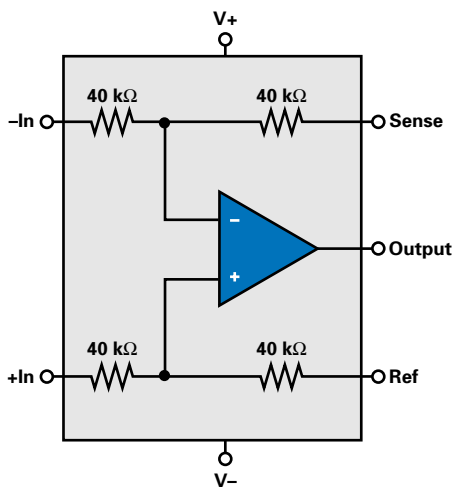


The difference amplifier is a moderate input impedance, closed-loop, fixed-gain block that allows the acquisition of signals in the presence of ground loops and noise. These devices can be used in a variety of circuit applications—precision, general-purpose, audio, low-power, high-speed and high-common-mode voltage applications.

## Difference Amplifier

The basic difference amplifier employs an op amp and four on-chip precision, laser-trimmed resistors. The INA132, for example, operates on 2.7-V to 36-V supplies and consumes only 160  $\mu$ A. It has a differential gain of 1 and high common-mode rejection. The output signal can be offset by applying a voltage to the Ref pin. The output sense pin can be connected directly at the load to reduce gain error. Because the resistor network divides down the input voltages, difference amplifiers can operate with input signals that exceed the power supplies.

INA132 Block Diagram



## High-Common-Mode Voltage Difference Amplifier Topology

A five-resistor version of the simple difference amplifier results in a device that can operate with very high levels of common-mode voltage—far beyond its power supply rails. For example, the INA117 can sense differential signals in the presence of common-mode voltages as high as  $\pm 200$  V while being powered from  $\pm 15$  V. This device is very useful in measuring

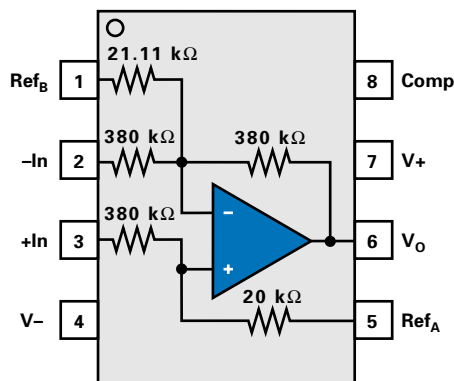
## Should I use a Difference or Instrumentation Amplifier?

Difference amplifiers excel when measuring signals with common-mode voltages greater than the power supply rails, when there is a low power requirement, when a small package is needed, when the source impedance is low or when a low-cost differential amp is required. The difference amp is a building block of the instrumentation amp.

Instrumentation amps are designed to amplify low-level differential signals in the presence of high-common-mode voltage. Generally, using an adjustable gain block, they are well suited to single-supply applications. The three-op-amp topology works well down to Gain = 1, with a performance advantage in AC CMR. The two-op-amp topology is appropriate for tasks requiring a small package footprint and a gain of 5 or greater. It is the best choice for low-voltage, single-supply applications.

current from a high-voltage power supply through a high-side shunt resistor.

INA117 Block Diagram



## Design Considerations

**Power supply**—common-mode voltage is always a function of the supply voltage. The INA103 instrumentation amplifier is designed to operate on voltage supplies up to  $\pm 25$  V, while the INA122 difference amp can be operated from a 2.2-V supply.

**Output voltage swing**—lower supply voltage often drives the need to maximize dynamic range by swinging close to the rails.

**Common-mode input voltage range (CMV)**—selection of the most suitable difference amp begins with an understanding of the input voltage range. Some offer resistor networks that divide down the input voltages, allowing operation with input signals that exceed the power

supplies. A five-resistor version of the simple difference amplifier results in a device that can operate with very high levels of common-mode voltage—far beyond the supply rails.

**Gain**—signal amplification needed for desired circuit function must be considered. With the uncommitted on chip op amp the INA145 and the INA146 can be configured for gains of 0.1 to 1000.

**Sensor impedance**—should be less than  $1/1000$  of difference amp impedance to retain CMR and gain accuracy. In other words, the amp input impedance should be 1,000 times higher than the source impedance.

**Offset voltage drift ( $\mu$ V/ $^{\circ}$ C)**—input offset voltage changes over temperature. This is more critical in applications with changing ambient temperature.

**Quiescent current**—often of high importance in battery-powered applications, where amplifier power consumption can greatly influence battery life.


**Slew rate**—if the signal is reporting a temperature, force or pressure, slew rate is not generally of great concern. If the signal is for an electronic event, (e.g. current, power output) a fast transition is needed.

**Common-mode rejection**—a measure of unwanted signal rejection and the amp's ability to extract a signal from surrounding DC, power line or other electrical noise.

## Difference Amplifiers Selection Guide

Device	Description	Ch.	Gain	Offset ( $\mu\text{V}$ ) (max)	Offset Drift ( $\mu\text{V}/^\circ\text{C}$ ) (max)	CMRR (dB) (min)	BW (MHz) (typ)	Output Voltage Swing (V) (min)	Power Supply (V)	$I_Q$ Per Ch. (mA) (max)	Package(s)	Price <sup>1</sup>
<b>General Purpose</b>												
INA132	Micropower, High Precision	1	1	250	5	76	0.3	(V+) – 1 to (V–) + 0.5	+2.7 to +36	0.185	DIP, SO	0.99
INA2132	Dual INA132	2	1	250	5	76	0.3	(V+) – 1 to (V–) + 0.5	+2.7 to +36	0.185	DIP, SO	0.99
INA133	High Precision, Fast	1	1	450	5	80	1.5	(V+) – 1.5 to (V–) + 1	$\pm 2.25$ to $\pm 18$	1.2	SOIC-8/-14	0.99
INA2133	Dual INA133	2	1	450	5	80	1.5	(V+) – 1.5 to (V–) + 1	$\pm 2.25$ to $\pm 18$	1.2	SOIC-8/-14	0.99
INA143	High Precision, G = 10 or 1/10	1	10, 1/10	250	3	86	0.15	(V+) – 1 to (V–) + 0.5	$\pm 2.25$ to $\pm 18$	1.2	SOIC-8/-14	0.99
INA2143	Dual INA143	2	10, 1/10	250	3	86	0.15	(V+) – 1 to (V–) + 0.5	$\pm 2.25$ to $\pm 18$	1.2	SOIC-8/-14	0.99
INA145	Resistor Programmable Gain	1	1-1000	1000	10	76	0.5	(V+) – 1 to (V–) + 0.5	$\pm 1.35$ to $\pm 18$	0.7	SOIC-8	1.40
INA2145	Dual INA145	2	1-1000	1000	10	76	0.5	(V+) – 1 to (V–) + 0.5	$\pm 1.35$ to $\pm 18$	0.7	SOIC-8	1.40
INA152	Micropower, High Precision	1	1	750	5	86	0.7	(V+) – 0.2 to (V–) + 0.2	+2.7 to +20	0.65	MSOP-8	1.10
INA154	High Speed, Precision, G = 1	1	1	750	20	80	3.1	(V+) – 2 to (V–) + 2	$\pm 4$ to $\pm 18$	2.9	SOIC-8	0.99
INA157	High Speed, G = 2 or 1/2	1	2, 1/2	500	20	86	4	(V+) – 2 to (V–) + 2	$\pm 4$ to $\pm 18$	2.9	SOIC-8	0.99
<b>Audio</b>												
INA134	Low Distortion: 0.0005%	1	1	1000	2	74	3.1	(V+) – 2 to (V–) + 2	$\pm 4$ to $\pm 18$	2.9	SOIC-8/-14	0.99
INA2134	Dual INA134	2	1	1000	2	74	3.1	(V+) – 2 to (V–) + 2	$\pm 4$ to $\pm 18$	2.9	SOIC-8/-14	0.99
INA137	Low Distortion, G = 1/2 or 2	1	2, 1/2	1000	2	74	4	(V+) – 2 to (V–) + 2	$\pm 4$ to $\pm 18$	2.9	SOIC-8/-14	0.99
INA2137	Dual INA137	2	2, 1/2	1000	2	74	4	(V+) – 2 to (V–) + 2	$\pm 4$ to $\pm 18$	2.9	SOIC-8/-14	0.99
<b>High-Common-Mode Voltage</b>												
INA117 <sup>2</sup>	$\pm 200$ -V CM Range	1	1	1000	20	86	0.2	(V+) – 5 to (V–) + 5	$\pm 5$ to $\pm 18$	2.0	SOIC-8	2.70
INA146	$\pm 100$ -V CM Range, Prog. Gain	1	0.1 to 100	5000	100	70	0.55	(V+) – 1 to (V–) + 0.1 5	$\pm 1.35$ to $\pm 18$	0.7	SOIC-8	1.60
INA148	$\pm 200$ -V CM Range, 1-M $\Omega$ Input	1	1	5000	100	70	0.1	(V+) – 1 to (V–) + 0.2 5	$\pm 1.35$ to $\pm 18$	0.3	SOIC-8	1.95
<b>High-Side Current Shunt Monitor</b>												
INA138	36 V max	1	200 $\mu\text{A}/\text{V}$	1000	1	100	0.8	0 to (V+) – 0.8	+2.7 to 36	0.045	SOT23-5	0.95
INA139	High Speed, 40 V max	1	1000 $\mu\text{A}/\text{V}$	1000	1	100	4.4	0 to (V+) – 0.9	+2.7 to 40	0.125	SOT23-5	0.95
INA168	60 V max	1	200 $\mu\text{A}/\text{V}$	1000	1	100	0.8	0 to (V+) – 0.8	+2.7 to 60	0.045	SOT23-5	1.15
INA169	High Speed, 60 V max	1	1000 $\mu\text{A}/\text{V}$	1000	1	100	4.4	0 to (V+) – 0.9	+2.7 to 60	0.125	SOT23-5	1.15
INA170	High-Side Bi-directional	1	1000 $\mu\text{A}/\text{V}$	1000	1	100	0.4	0 to (V+) – 0.9	+2.7 to 60	0.125	MSOP-8	1.21

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000. <sup>2</sup>–55 to +125 version available.

 The instrumentation amplifier (IA) is a high input impedance, closed-loop fixed- or adjustable-gain block that allows the amplification of low-level signals in the presence of common-mode errors and noise. TI offers many types of instrumentation amplifiers including single-supply, low-power, high-speed and low-noise devices. These instrumentation amplifiers are available in either the traditional three-op-amp or in the cost-effective two-op-amp topology.

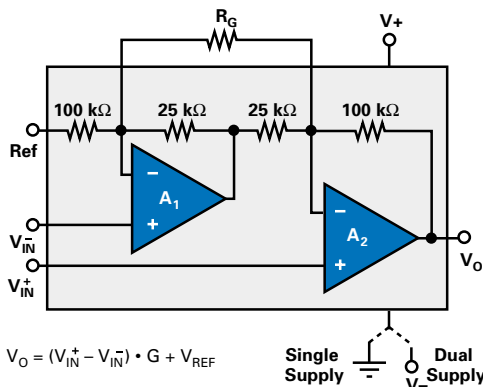
### Three-Op-Amp Version

The three-op-amp topology is the benchmark for instrumentation amplifier performance. These devices provide a wide gain range (down to  $G = 1$ ) and generally offer the highest performance. Symmetrical inverting and non-inverting gain paths provide better common-mode rejection at high frequencies. Some types use current-feedback-type input op amps which maintain excellent bandwidth in high gain.

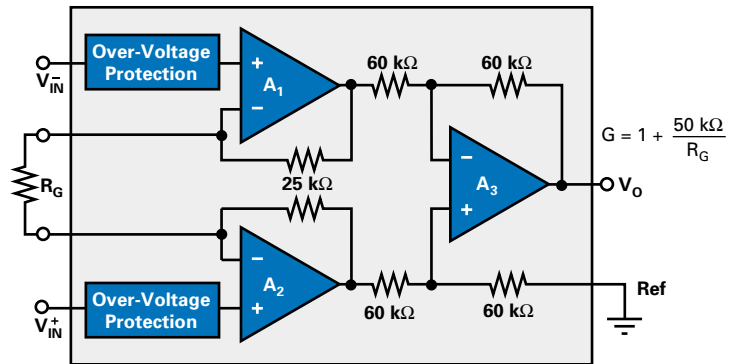
### Two-Op-Amp Version

The two-op-amp topology can provide wider common-mode voltage range, especially in low-voltage, single-supply applications. Their simpler internal circuitry allows lower cost, lower quiescent current and smaller package sizes. This topology, however, does not lend itself to gains less than four (INA125) or five (all others).

*Two-op-amp topology provides wider common-mode range in low-voltage, single-supply applications.*



*The three-op-amp topology is the benchmark for instrumentation amplifier performance.*



### Design Considerations

**Supply voltage**—TI has developed a series of low voltage, single-supply, rail-to-rail instrumentation amps suitable for a wide variety of applications requiring maximum dynamic signal range.

**Gain requirement**—for high-gain applications consider a low total noise device, as drift, input bias current and voltage offset all contribute to error.

**Common-mode voltage range**—the voltage input range over which the amplifier can operate and the differential pair behaves as a linear amplifier for differential signals.

**Input bias current**—can be an important factor in many applications, especially those sensing a low current or where the sensor impedance is very high. The INA116 requires only 3-fA ( $10^{-15}$ ) typical of input bias current.

**Offset voltage and drift**—IAs are generally used in high-gain applications, where any amp errors are amplified by the circuit gain. This can become a significant portion of the overall signal unless  $V_{OS}$  and drift are taken into account. Bipolar amps excel in limiting voltage errors related to offset and drift in low source impedance applications.

**Current-feedback vs. voltage-feedback input stage**—appropriate for designers needing higher bandwidth or a more consistent 3-dB rolloff frequency over various gain settings. The INA128 and INA129 provide a significantly higher 3-dB rolloff

frequency than voltage feedback input stage instrumentation amps and have a 3-dB rolloff at essentially the same frequency in both  $G = 1$  and  $G = 10$  configurations.

### Technical Information

Instrumentation amplifiers (IA) accurately output the difference between the input signals providing Common-Mode Rejection (CMR). It is the key parameter and main purpose for using this type of device. CMR measures the device's ability to reject signals that are common to both inputs.

IAs are often used to amplify the differential output of a bridge sensor, amplifying the tiny bridge output signals while rejecting the large common-mode voltage. They provide excellent accuracy and performance, yet require minimal quiescent current. Gain is usually set with a single external resistor.

In some applications unwanted common-mode signals may be less conspicuous. Real-world ground interconnections are not perfect. What may, at first, seem to be a viable single-ended amplifier application can become an accumulation of errors. Error voltages caused by currents flowing in ground loops sum with the desired input signal and are amplified by a single-ended input amp. Even very low impedance grounds can have induced voltages from stray magnetic fields. As accuracy requirements increase, it becomes more difficult to design accurate circuits with a single-ended input amplifier. The differential input instrumentation amplifier is the answer.

## Single-Supply Instrumentation Amplifiers Selection Guide

Device <sup>1</sup>	Description	Gain	Non Linearity (%) (max)	Input Bias Current (nA) (max)	Offset at G = 100 (μV) (max)	Offset Drift (μV/°C) (max)	CMRR at G = 100 (dB) (min)	BW at G = 100 (kHz) (min)	Noise 1 kHz (nV/√Hz) (typ)	Power Supply (V)	I <sub>Q</sub> per Amp (mA) (max)	Package(s)	Price <sup>2</sup>
<b>Single-Supply, Low Power I<sub>Q</sub> &lt; 525 μA per Instrumentation Amp</b>													
INA321	RRO, SHDN, Low Offset and Gain Error, Wide Temp	5 to 10000	0.01	0.01	1000	7 <sup>3</sup>	90	50	100	2.7 to 5.5	0.06	MSOP-8	1.10
INA2321	Dual INA321	5 to 10000	0.01	0.01	1000	7 <sup>3</sup>	90	50	100	2.7 to 5.5	0.06	TSSOP-14	2.02
INA322	RRO, SHDN, Wide Temp, Low Cost	5 to 10000	0.01	0.01	10000	7	60	50	100	2.7 to 5.5	0.06	MSOP-8	0.91
INA2322	Dual INA322	5 to 10000	0.01	0.01	10000	7	60	50	100	2.7 to 5.5	0.06	TSSOP-14	1.72
INA122	μPower, RRO, CM to Gnd	5 to 10000	0.012	25	250	3	90	5	60	2.2 to 36	0.085	DIP-8, SOIC-8	1.95
INA332	RRO, Wide BW, SHDN, Wide Temp, Low Cost	5 to 1000	0.01	0.01	10000	7 <sup>3</sup>	60	500	100	2.7 to 5.5	0.1	MSOP-8	0.80
INA2332	Dual INA332	5 to 1000	0.01	0.01	10000	7 <sup>3</sup>	60	500	100	2.7 to 5.5	0.1	MSOP-8	1.45
INA126	μPower, < 1 V V <sub>SAT</sub> , Low Cost	5 to 10000	0.012	25	250	3	83	9	35	2.7 to 36	0.2	DIP/SO/MSOP-8	0.99
INA2126	Dual INA126	5 to 10000	0.012	25	250	3	83	9	35	2.7 to 36	0.2	DIP/SO/MSOP-16	1.80
INA118	Precision, Low Drift, Low Power <sup>4</sup>	1 to 10000	0.002	5	55	0.7	107	70	10	2.7 to 36	0.385	DIP-8, SOIC-8	3.73
INA331	RRO, Wide BW, SHDN, Wide Temp	5 to 1000	0.01	0.01	500	5 <sup>3</sup>	90	2000	46	2.7 to 5.5	0.5	MSOP-8	1.05
INA2331	Dual INA331	5 to 1000	0.01	0.01	1000	5 <sup>3</sup>	80	2000	46	2.7 to 5.5	0.5	TSSOP-14	2.35
INA125	Internal Ref, Sleep Mode <sup>4</sup>	4 to 10000	0.01	25	250	2	100	4.5	38	2.7 to 36	0.525	DIP-8, SOIC-16	2.10
<b>Single-Supply, Low Input Bias Current I<sub>B</sub> &lt; 100 pA</b>													
INA155	Low Offset, RRO, Wide Temp, SR = 6.5 V/μs	10, 50	0.015	0.01	1000	5 <sup>3</sup>	86	110	40	2.7 to 5.5	2.1	MSOP-8	1.00
INA156	Low Offset, RRO, Low Cost, Wide Temp, SR = 6.5 V/μs	10, 50	0.015	0.01	8000	5 <sup>3</sup>	86	110	40	2.7 to 5.5	2.10	SOIC-8, MSOP-8	0.90
INA321	RRO, SHDN, Low Offset and Gain Error, Wide Temp	5 to 10000	0.01	0.01	1000	7 <sup>3</sup>	90	50	100	2.7 to 5.5	0.06	MSOP-8	1.10
INA2321	Dual INA321	5 to 10000	0.01	0.01	1000	7 <sup>3</sup>	90	50	100	2.7 to 5.5	0.06	TSSOP-14	2.02
INA322	RRO, SHDN, Wide Temp, Low Cost	5 to 10000	0.01	0.01	10000	7	60	50	100	2.7 to 5.5	0.06	MSOP-8	0.91
INA2322	Dual INA322	5 to 10000	0.01	0.01	10000	7	60	50	100	2.7 to 5.5	0.06	TSSOP-14	1.72
INA331	RRO, Wide BW, SHDN, Wide Temp	5 to 1000	0.01	0.01	500	5 <sup>3</sup>	90	2000	46	2.7 to 5.5	0.5	MSOP-8	1.05
INA2331	Dual INA331	5 to 1000	0.01	0.01	1000	5 <sup>3</sup>	80	2000	46	2.7 to 5.5	0.5	TSSOP-14	2.35
INA332	RRO, Wide BW, SHDN, Wide Temp, Low Cost	5 to 1000	0.01	0.01	10000	7 <sup>3</sup>	60	500	100	2.7 to 5.5	0.1	MSOP-8	0.80
INA2332	Dual INA332	5 to 1000	0.01	0.01	10000	7 <sup>3</sup>	60	500	100	2.7 to 5.5	0.1	TSSOP-14	1.45
<b>Single-Supply, Precision V<sub>OS</sub> &lt; 300 μV, Low V<sub>OS</sub> Drift</b>													
INA118	Precision, Low Drift, Low Power <sup>4</sup>	1 to 10000	0.002	5	55	0.7	107	70	10	2.7 to 36	0.385	DIP-8, SOIC-8	3.73
<b>INA326</b>	RRIO, Auto Zero, CM > Supply, Low Drift	0.1 to 10000	0.01	2	100	0.4	100	1	33	2.7 to 5.5	3.4	MSOP-8	1.70
<b>INA327</b>	RRIO, Auto Zero, SHDN, CM > Supply, Low Drift	0.1 to 10000	0.01	2	100	0.4	100	1	33	2.7 to 5.5	3.4	MSOP-10	1.85
<b>INA337</b>	RRIO, Auto Zero, Low Drift, CM > Supply, Wide Temp	0.1 to 10000	0.01	2	100	0.4	106	1	33	2.7 to 5.5	3.4	MSOP-8	1.71
<b>INA338</b>	RRIO, Auto Zero, Low Drift, CM > Supply, SHDN, Wide Temp	0.1 to 10000	0.01	2	100	0.4	106	1	33	2.7 to 5.5	3.4	MSOP-10	1.85
INA122	μPower, RRO, CM to Gnd	5 to 10000	0.012	25	250	3	90	5	60	2.2 to 36	0.085	DIP-8, SOIC-8	1.95
INA125	Internal Ref, Sleep Mode <sup>4</sup>	4 to 10000	0.01	25	250	2	100	4.5	38	2.7 to 36	0.525	DIP-8, SOIC-16	2.10
INA126	μPower, < 1 V V <sub>SAT</sub> , Low Cost	5 to 10000	0.012	25	250	3	83	9	35	2.7 to 36	0.2	DIP/SO/MSOP-8	0.99
INA2126	Dual INA126	5 to 10000	0.012	25	250	3	83	9	35	2.7 to 36	0.2	DIP/SO/MSOP-16	1.80
<b>Signal Amplifiers for Temperature Control</b>				<b>I<sub>B</sub> (nA)</b>	<b>Temp Error<sup>5</sup></b>			<b>% Noise</b>					
<b>INA330</b>	Optimized for Precision 10 K Thermistor Applications	—	—	0.2 <sup>3</sup>	—	0.009°C <sup>3</sup>	—	1	0.0001 °C pp <sup>3</sup>	2.7 to 5.5	3.6	MSOP-10	1.45

<sup>1</sup>New products appear in **BOLD RED**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000. <sup>3</sup>Typical. <sup>4</sup>Internal +40-V input protection. <sup>5</sup>-40°C to +85°C.

## Dual-Supply Instrumentation Amplifiers Selection Guide

Device	Description	Gain	Non Linearity (%) (max)	Input Bias Current (nA) (max)	Offset at G = 100 ( $\mu$ V) (max)	Offset Drift ( $\mu$ V/ $^{\circ}$ C) (max)	CMRR at G = 100 (dB) (min)	BW at G = 100 (kHz) (min)	Noise 1 kHz ( $n$ V/ $\sqrt{Hz}$ ) (typ)	Power Supply (V)	$I_Q$ per Amp (mA) (max)	Package(s)	Price <sup>1</sup>
<b>Dual-Supply, Low Power <math>I_Q &lt; 850 \mu</math>A per Instrumentation Amp</b>													
INA122	$\mu$ power, RRO, CM to Gnd	5 to 10000	0.012	25	250	3	90	5	60	$\pm 1.3$ to $\pm 18$	0.085	DIP-8, SOIC-8	1.95
INA126 <sup>4</sup>	$\mu$ power, $< 1 V V_{SAT}$ , Low Cost	5 to 10000	0.012	25	250	3	83	9	35	$\pm 1.35$ to $\pm 18$	0.2	DIP/SO/MSOP-8	0.99
INA118	Precision, Low Drift, Low Power <sup>2</sup>	1 to 10000	0.002	5	55	0.7	107	70	10	$\pm 1.35$ to $\pm 18$	0.385	DIP-8, SOIC-8	3.73
INA121	Low Bias, Precision, Low Power <sup>2</sup>	1 to 10000	0.005	0.05	500	5	100	50	20	$\pm 2.25$ to $\pm 18$	0.525	DIP-8, SO-8	2.35
INA125	Internal Ref, Sleep Mode <sup>2</sup>	4 to 10000	0.01	25	250	2	100	4.5	38	$\pm 1.35$ to $\pm 18$	0.525	DIP-8, SOIC-16	2.10
INA128 <sup>4</sup>	Precision, Low Noise, Low Drift <sup>2</sup>	1 to 10000	0.002	5	60	0.7	120	200	8	$\pm 2.25$ to $\pm 18$	0.8	DIP-8, SOIC-8	3.31
INA129	Precision, Low Noise, Low Drift, AD620 Second Source <sup>2</sup>	1 to 10000	0.002	5	60	0.7	120	200	8	$\pm 2.25$ to $\pm 18$	0.8	DIP-8, SOIC-8	3.31
INA141 <sup>4</sup>	Precision, Low Noise, Low Power, Pin Com. w/AD6212 <sup>2</sup>	10, 100	0.002	5	50	0.7	110	200	8	$\pm 2.25$ to $\pm 18$	0.8	DIP-8, SOIC-8	3.31
<b>Dual-Supply, Low Input Bias Current <math>I_B &lt; 100 \mu</math>A</b>													
INA110	Fast Settle, Low Noise, Wide BW	1,10,100, 200, 500	0.01	0.05	280	2.5	106	470	10	$\pm 6$ to $\pm 18$	4.5	CDIP-16	6.70
INA121	Precision, Low Power <sup>2</sup>	1 to 10000	0.005	0.05	500	5	100	50	20	$\pm 2.25$ to $\pm 18$	0.525	DIP-8, SO-8	2.35
INA111	Fast Settle, Low Noise, Wide BW	1 to 10000	0.005	0.02	520	6	106	450	10	$\pm 6$ to $\pm 18$	4.5	DIP-8, SO-16	3.91
INA116	Ultra Low $I_B$ 3 fA (typ), with Buffered Guard Drive Pins <sup>2</sup>	1 to 10000	0.01	0.0001	5000	40	80	70	28	$\pm 4.5$ to $\pm 18$	1.4	DIP-16, SO-16	3.95
<b>Dual-Supply, Precision <math>V_{OS} &lt; 300 \mu</math>V, Low <math>V_{OS}</math> Drift</b>													
INA114	Precision, Low Drift <sup>2</sup>	1 to 10000	0.002	2	50	0.25	110	10	11	$\pm 2.25$ to $\pm 18$	3	DIP-8, SO-16	3.55
INA115	Precision, Low Drift, with Gain Sense Pins <sup>2</sup>	1 to 10000	0.002	2	50	0.25	120	10	11	$\pm 2.25$ to $\pm 18$	3	SO-16	4.00
INA131	Low Noise, Low Drift <sup>2</sup>	100	0.002	2	50	0.25	110	70	12	$\pm 2.25$ to $\pm 18$	3	DIP-8	3.59
INA141 <sup>4</sup>	Precision, Low Noise, Low Power, Pin Com. w/AD6212 <sup>2</sup>	10, 100	0.002	5	50	0.7	110	200	8	$\pm 2.25$ to $\pm 18$	0.8	DIP-8, SOIC-8	3.31
INA118	Precision, Low Drift, Low Power <sup>2</sup>	1 to 10000	0.002	5	55	0.7	107	70	10	$\pm 1.35$ to $\pm 18$	0.385	DIP-8, SOIC-8	3.73
INA128 <sup>4</sup>	Precision, Low Noise, Low Drift <sup>2</sup>	1 to 10000	0.002	5	60	0.7	120	200	8	$\pm 2.25$ to $\pm 18$	0.8	DIP-8, SOIC-8	3.31
INA129	Precision, Low Noise, Low Drift, AD620 Second Source <sup>2</sup>	1 to 10000	0.002	5	60	0.7	120	200	8	$\pm 2.25$ to $\pm 18$	0.8	DIP-8, SOIC-8	3.31
INA122	$\mu$ power, RRO, CM to Gnd	5 to 10000	0.012	25	250	3	90	5	60	$\pm 1.3$ to $\pm 18$	0.085	DIP-8, SOIC-8	1.95
INA125	Internal Ref, Sleep Mode <sup>2</sup>	4 to 10000	0.01	25	250	2	100	4.5	38	$\pm 1.35$ to $\pm 18$	0.525	DIP-8, SOIC-16	2.10
INA126 <sup>4</sup>	$\mu$ power, $< 1 V V_{SAT}$ , Low Cost	5 to 10000	0.012	25	250	3	83	9	35	$\pm 1.35$ to $\pm 18$	0.2	DIP/SO/MSOP-8	0.99
INA101	Low Noise, Wide BW, Gain Sense Pins, Wide Temp	1 to 10000	0.007	30	259	23	100	25000	13	$\pm 5$ to $\pm 18$	8.5	T0-100, CDIP-14, PDIP-14, SO-16	7.52
INA110	Fast Settle, Low Noise, Low Bias, Wide BW	1,10,100, 200, 500	0.01	0.05	280	2.5	106	470	10	$\pm 6$ to $\pm 18$	4.5	CDIP-16	6.70
<b>Dual-Supply, Lowest Noise</b>													
INA103	Precision, Fast Settle, Low Drift, Audio, Mic Pre Amp, THD+N = 0.0009%	1, 100	0.0006 <sup>3</sup>	12000	255	1.2 <sup>3</sup>	100	800	1	$\pm 9$ to $\pm 25$	13	DIP-16, SO-16	4.65
INA163	Precision, Fast Settle, Low Drift, Audio, Mic Pre Amp, THD+N = 0.002%	1 to 10000	0.0006 <sup>3</sup>	12000	300	1.2 <sup>3</sup>	100	800	1	$\pm 4.5$ to $\pm 18$	12	SOIC-14	1.95
INA166	Precision, Fast Settle, Low Drift, Audio, Mic Pre Amp, THD+N = 0.09%	2000	0.005	12000	300	2.5 <sup>3</sup>	100	450	1.3	$\pm 4.5$ to $\pm 18$	12	SO-14 Narrow	5.66
INA217	Precision, Low Drift, Audio, Mic PreAmp, THD+N = 0.09% SSM2017 Replacement	1 to 10000	0.0006 <sup>3</sup>	12000	300	1.2 <sup>3</sup>	-100	800	1.3	$\pm 4.5$ to $\pm 18$	12	DIP-8, SO-16	2.35

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000. <sup>2</sup>Internal +40-V input protection. <sup>3</sup>Typical. <sup>4</sup>Parts also available in a dual version.



# Digitally Programmable Gain Amplifiers

Programmable gain instrumentation amplifiers (PGA) are extremely versatile data acquisition input amplifiers that provide digital control of gain for improved accuracy and extended dynamic range. Many have inputs that are protected to  $\pm 40$  V even with the power supply off. A single input amplifier type can be connected to a variety of sensors or signals. Under processor control, the switched gain extends the dynamic range of the system.

All PGA-series amps have TTL- or CMOS-compatible inputs for easy microprocessor interface. Inputs are laser trimmed for low offset voltage and low drift to allow use without the need of external components.

## Design Considerations

### Primary

**Digitally selected gain required**—two pins allow the selection of up to four different gain states. A PGA202 and PGA203 can be put in series for greater gain selection.

**Non-linearity (accuracy)**—depends heavily on what is being fed. A 16-bit converter will require significantly better accuracy (i.e. lower non-linearity) than a 10-bit converter.

### Secondary

**Gain error and drift**—for higher gain, high-precision applications will require closer attention to drift and gain error.

**Input bias current**—DC input current needed at each amplifier input to give 0-V out when input offset voltage is zero. High source impedance applications generally require FET-input amps, which minimize bias current errors by requiring extremely low bias current.

## Technical Information

The PGA206 provides binary gain steps of 1, 2, 4 and 8 V/V, selected by CMOS- or TTL-compatible inputs. The PGA207 has gains of 1, 2, 5 and 10 V/V, adding a full decade to the system dynamic range. The low input bias current, FET-input stage assures that series resistance of the multiplexer does not introduce errors. Fast

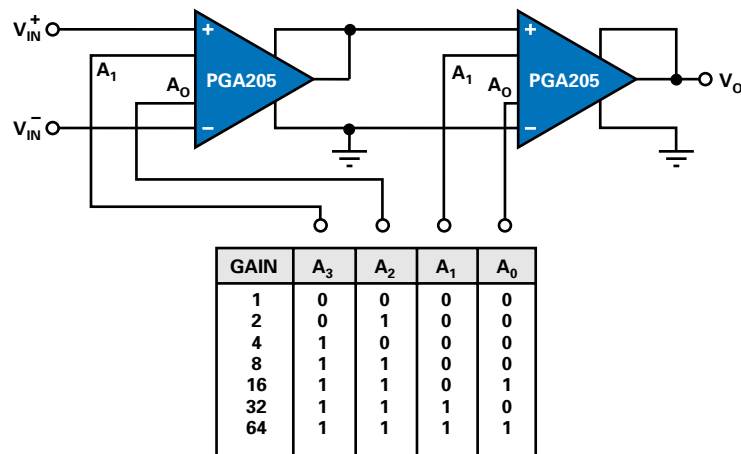
settling time (3.5  $\mu$ s to 0.01%) allows fast polling of many channels.

The PGA204 and PGA205 have precision bipolar input stages especially well suited to low-level signals. The PGA205 has gain steps of 1, 2, 4 and 8.

## Typical Applications

- Data acquisition
- Auto-ranging circuits
- Remote instrumentation
- Test equipment
- Medical/physiological instrumentation
- General analog interface boards

Connecting two programmable gain amps can provide binary gain steps  $G = 1$  to  $G = 64$ .



## Digitally Programmable Gain Amplifiers Selection Guide

Device	Description	Gain	Non Linearity at G = 100 (%) (max)	Offset ( $\mu$ V) (max)	Offset Drift ( $\mu$ V/ $^{\circ}$ C) (max)	CMRR at G = 100 (dB) (min)	BW at G = 100 (kHz) (typ)	Noise at 1kHz ( $n$ V/ $\sqrt{Hz}$ ) (typ)	Power Supply (V)	I <sub>0</sub> (mA) (max)	Package(s)	Price <sup>1</sup>
3606	High-Resolution Hybrid	1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024	0.01	22	1	100	40	30	$\pm 8$ to $\pm 18$	10	Module-32	201.12
PGA103	Precision, Single-Ended Input	1, 10, 100	0.01	500	2 (typ)	—	250	11	$\pm 4.5$ to $\pm 18$	3.5	SOL-8	3.90
PGA202	High Speed, FET-Input, 50-pA I <sub>B</sub>	1, 10, 100, 1000	0.012	1000	12	92	1000	12	$\pm 4.5$ to $\pm 18$	6.5	DIP-14	7.28
PGA203	High Speed, FET-Input, 50-pA I <sub>B</sub>	1, 2, 4, 8	0.012	1000	12	92	1000	12	$\pm 4.5$ to $\pm 18$	6.5	DIP-14	7.28
PGA204	High Precision, Gain Error: 0.25% <sup>2</sup>	1, 10, 100, 1000	0.002	50	0.25	110	10	13	$\pm 4.5$ to $\pm 18$	5.2	SOL-16	6.82
PGA205	Gain Drift: 0.024 ppm/ $^{\circ}$ C <sup>2</sup>	1, 2, 4, 8	0.002	50	0.25	95	100	15	$\pm 4.5$ to $\pm 18$	5.2	SOL-16	6.82
PGA206	High Speed, FET-Input <sup>2</sup> , 100-pA I <sub>B</sub>	1, 2, 4, 8	0.002	1500	2 (typ)	95	600	18	$\pm 4.5$ to $\pm 18$	12.4	DIP-16, SOL-16	10.13
PGA207	High Speed, FET-Input <sup>2</sup> , 100-pA I <sub>B</sub>	1, 2, 5, 10	0.002	1500	2 (typ)	95	600	18	$\pm 4.5$ to $\pm 18$	12.4	DIP-16, SOL-16	11.14

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000. <sup>2</sup>Internal +40-V input protection.

# Voltage-Controlled Gain Amplifiers

The voltage-controlled gain amplifier (VCA) provides linear-dB gain and gain-range control with high impedance inputs. Available in single and dual configurations, the VCA series is designed to be used as a flexible gain-control element in a variety of electronic systems. With a broad gain-control range, both gain and attenuation control are provided for maximum flexibility.

## Design Considerations

### Primary

**Input frequency**—VCA series capable of processing input frequencies up to 20 MHz.

**Noise ( $nV/\sqrt{Hz}$ )**—as low as  $1 nV/\sqrt{Hz}$  total noise (max).

**Variable gain range**—to 45 dB for VCA261x series, 77 dB for VCA610.

### Secondary

**Number of channels**—VCA610 is single channel; VCA261x are all dual channel.

**Distortion**—low second-harmonic distortion ( $-40$  dB min) with low crosstalk (70 dB at max gain, 5 MHz).

or turn-off where abrupt gain changes can create artifacts and other errors.

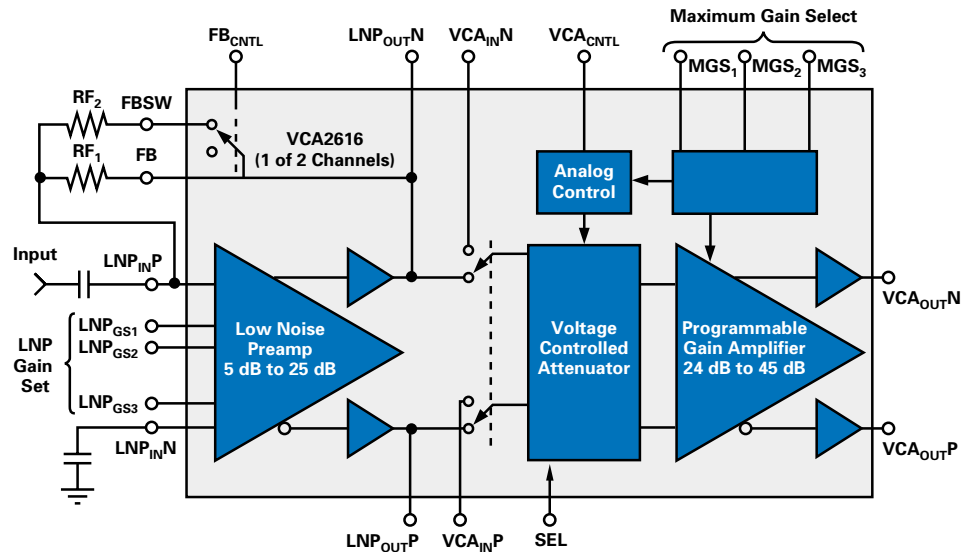
## Technical Information

The broad attenuation range can be used for gradual or controlled channel turn-on

## Typical Applications

- Ultrasound systems
- Wireless receivers
- Test equipment

VCA2616 Block Diagram



## Voltage-Controlled Gain Amplifiers Selection Guide

Device	$V_N$ ( $nV/\sqrt{Hz}$ )	Bandwidth (MHz) (typ)	Specified at $V_S$ (V)	Number of Channels	Variable Gain Range (dB)	Package(s)	Price <sup>1</sup>
VCA2612	1.25	40	5	2	45	TQFP	11.90
VCA2613	1	40	5	2	45	TQFP	9.75
VCA2614	4.8	40	5	2	40	TQFP	7.95
VCA2616	1	40	5	2	45	TQFP	9.75
VCA610	2.2	1	5	1	77	SOIC	11.12
VCA2618	5.5	40	5	2	45	TQFP	7.95
THS7530	1.27	300	5	1	46	PowerPAD™	3.65

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

# Audio Amplifiers

Consumers are enjoying new ways to listen to music, books and news, while demanding more flexibility, better quality and multi-function products. There is an ever-increasing demand for high-end entertainment for the everyday consumer. The market expects the best listening experience from any audio format and source, mobile or stationary and at a competitive price.

By offering flexible, cost-efficient, end-to-end audio solutions, TI provides OEMs/ODMs with faster time to market and one-stop shopping. TI's complete audio solutions include best-in-class silicon, systems expertise, software and support. By leveraging the programmability, performance headroom and design flexibility of TI's leading DSP and analog technologies, customers have the ability to build audio products with more functionality that offer a true, lifelike sound experience at a lower overall system cost.

## Design Considerations

### Primary

**Output power**—supply voltage and load impedance limit the level of output power (i.e. volume) an audio power amp (APA) can drive. Always verify that the desired output power is theoretically possible with the equation

$$P_O = \frac{V_O^2}{R_L}$$

where  $V_O$  is the RMS voltage of the output signal and  $R_L$  is the load impedance.

**Output configuration**—there are two types of output configurations, single-ended (SE) and bridge-tied load (BTL). An SE configuration is where one end of the load is connected to the APA and the other end of the load is connected to ground. Used primarily in headphone applications or where the audio power amplifier and

## Points to Consider When Choosing an Audio Power Amplifier (APA)

- Is the APA driving speakers or headphones?
- What is the impedance of the headphones or speakers: 4  $\Omega$ , 8  $\Omega$ , 32  $\Omega$ ?
- Is the application stereo, mono or multichannel?
- Is the supply voltage  $\leq 3$  V, 5 V, 12 V or  $\geq 18$  V?
- What is the required output power?
- Is there a need for volume control?
- Is the APA input single-ended or differential?

Digital audio power amplifiers require unique considerations. The latest information is located at [www.ti.com/digitalaudioapps.html](http://www.ti.com/digitalaudioapps.html).

speaker are in different enclosures. A BTL configuration is where both ends of the load are connected to an APA. This configuration effectively quadruples the output power capability of the system, and is used primarily in applications that are space constrained and where the APA and speaker are in the same enclosure.

**Total Harmonic Distortion + Noise**—harmonic distortion is distortion at frequencies that are whole number multiples of the test tone frequency. THD+N is typically specified for rated output power at 1 kHz. Values below 0.5 percent to 0.3 percent are negligible to the untrained ear.

**Amplifier technology (Class-D and Class-AB)**—Class-D and Class-AB are the most common APAs in consumer electronics, because of their great performance and low cost. Class-D amps are very efficient and provide the longest battery life and lowest heat dissipation. Class-AB amps offer the greatest selection of features (e.g. digital volume control and bass boost).

### Secondary

**Digital volume control**—this input changes the gain of the APA when digital high or low pulses are applied to the UP and DOWN pins.

**DC volume control**—internal gain settings that are controlled by the VOLUME pin.

**Integrated gain settings**—the internal gain settings are controlled via the input pins GAIN0 and GAIN1.

**DEPOP**—circuitry internal to the APA. It minimizes voltage spikes when the APA turns on, off or transitions in or out of shutdown mode.

**MUX**—allows two different audio sources to the APA that are controlled independently of the amplifier configuration.

**Shutdown**—circuitry that places the APA in a very-low-power consumption standby state.

## Technical Information

TI APAs are easy to design with requiring only a few external components.

**Power supply capacitors**— $C_{VDD}$  minimizes THD by filtering off the low frequency noise and the high frequency transients.

**Input capacitors**—in the typical application an input capacitor,  $C_{IN}$ , is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation.  $C_{IN}$  is usually in the 0.1  $\mu$ F to 10  $\mu$ F range for good low-frequency response.

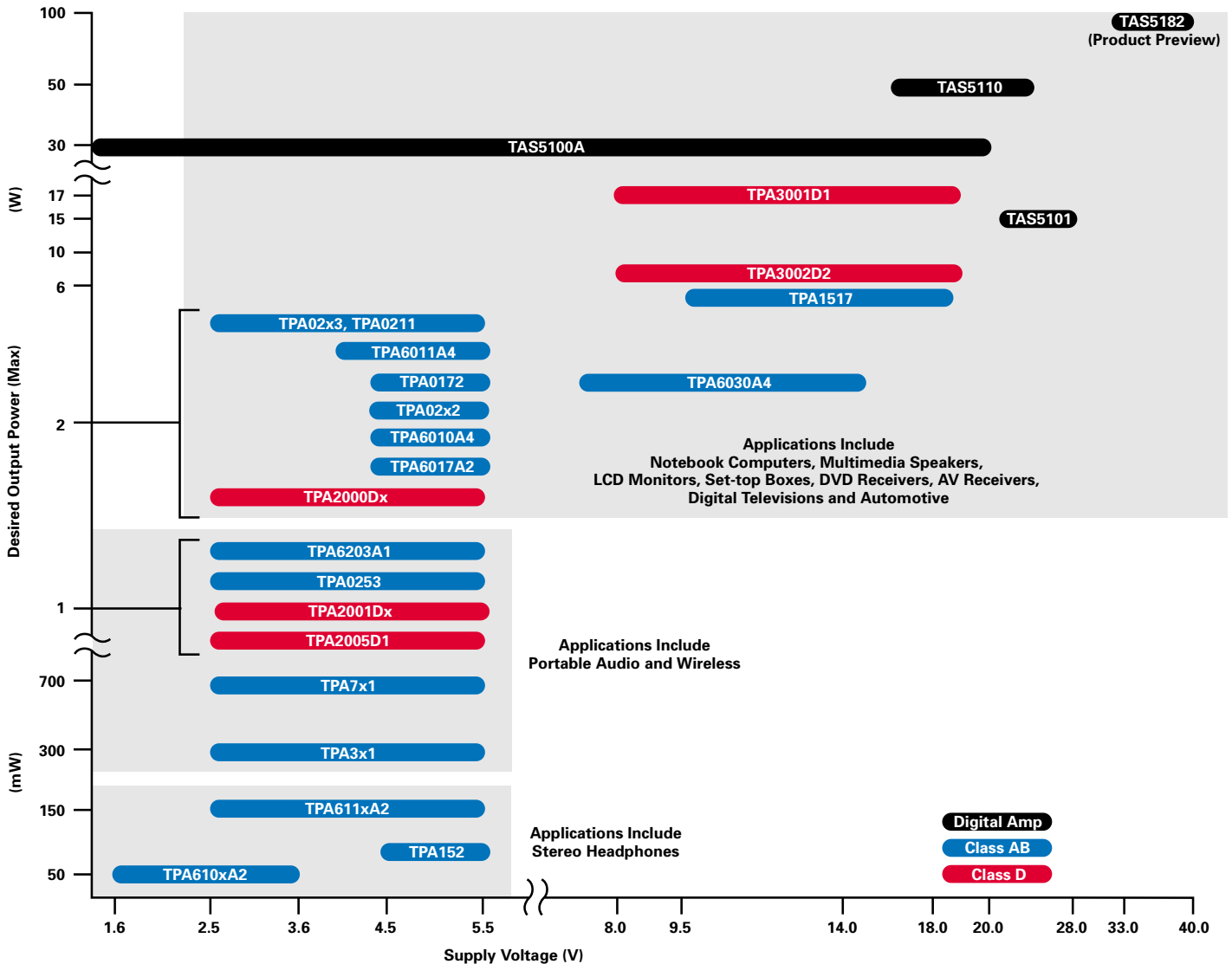
**Bypass capacitor**— $C_{\text{BYPASS}}$  controls the start up time and helps to reduce the THD. Typically this capacitor is ten times larger than the input decoupling capacitors ( $C_{\text{IN}}$ ).

**Layout**—by respecting basic rules, Class-D amplifiers' layout can be made

easy. Decoupling caps must be close to the device, the output loop must be small to avoid the use of a filter and the differential input traces must be kept together to limit the RF rectification. Analog  $V_{\text{DD}}$  and switching  $V_{\text{DD}}$  need to be separated back to the supply source.

**Migration path**—APA products are in a constant evolution moving from Class-AB mono speaker drivers to optimized stereo Class-D amplifiers with advanced features. The latest generation is the most cost effective for the application.

## Audio Power Amplifiers Product Portfolio Overview



Device <sup>1</sup>	Description	Stereo/ Mono Speaker Drive	Stereo/ Mono Head- phone Drive	Output Power (W)	V <sub>CC</sub> (V) (min)	V <sub>DD</sub> (V) (max)	THD+N at 1 kHz (%)	PSRR (dB)	I <sub>Q</sub> Per Ch. (mA) (typ)	I <sub>SD</sub> (μA)	Min Load Impe- dence (Ω)	Input MUX	Depop	Mute	SHDN (Active Low/ High)	Int. Gain	DC Volume Control	Digital Volume Control	Package(s)	Package Symbol- ization	Price <sup>2</sup>
<b>TPA3001D1</b>	Mono, Class-D, Differential Input	M	—	20	8	18	0.1	70	8	1	4	—	✓	—	L	✓	—	—	TSSOP	TPA3000D1	2.82
<b>TPA3002D2</b>	Stereo, Class-D, Differential Input	S	7	8	14	0.5	60	8	1	4	—	—	✓	—	L	✓	✓	—	PHP	TPA3002D2	3.49
TPA032D02	Stereo, Class-D, Differential Input	S	—	10	8	14	0.5	40	12.5	20	4	—	—	✓	L	—	—	—	TSSOP	TPA032D02	3.45
TPA032D03	Mono, Class-D, Differential Input and Class-AB Headphone Amp with Depop	M	S	10	8	14	0.5	40	12.5	20	4	—	—	✓	L	—	—	—	TSSOP	TPA032D03	3.27
TPA032D04	Stereo, Class-D, Differential Inputs and Class-AB Headphone Amp with Depop	S	S	10	8	14	0.5	40	12.5	20	4	—	—	✓	L	—	—	—	TSSOP	TPA032D04	3.60
TPA1517	Stereo, Single-Ended Speaker Driver	S	—	6	9.5	18	10	65	22.5	7	4	—	—	✓	L	—	—	—	SOIC, DIP	TPA1517	0.79
<b>TPA6030A4</b>	Stereo, Headphone Driver, High Supply Voltage	S	S	3	7	15	0.06	60	18	1	16	✓	✓	—	L	—	✓	—	TSSOP	TPA6030A4	1.33
TPA0172	Stereo, Headphone Drive, I <sup>2</sup> C Control	S	S	2	4.5	5.5	0.15	75	4	15	4	✓	✓	✓	L	—	—	✓	TSSOP	TPA0172	2.51
TPA0211	Mono, Earphone Drive	M	M	2	2.5	5.5	0.2	75	4	1	4	—	✓	—	L	—	—	—	MSOP	AEG	0.67
TPA0212	Stereo, Headphone Drive, Optimized for Battery Life	S	S	2	4.5	5.5	0.75	77	3	150	3	✓	✓	—	L	✓	—	—	TSSOP	TPA0212	1.01
TPA0213	Mono, Headphone Drive, Mono Input, Optimized for Battery Life	M	S	2	2.5	5.5	0.2	75	3.6	1	4	✓	✓	—	L	—	—	—	MSOP	AEH	1.09
TPA0222	Stereo, Headphone Drive, Optimized for Fidelity	S	S	2	4.5	5.5	0.5	77	9	150	3	✓	✓	—	L	✓	—	—	TSSOP	TPA0222	1.01
TPA0223	Mono, Headphone Drive, Mono Input, Optimized for Fidelity	M	S	2	2.5	5.5	0.2	75	10	1	4	✓	✓	—	L	—	—	—	MSOP	AEI	1.09
TPA0232	Stereo, Headphone Drive, Optimized for Battery Life	S	S	2	4.5	5.5	0.4	67	5	150	3	✓	✓	—	L	—	✓	—	TSSOP	TPA0232	1.50
TPA0233	Mono, Headphone Drive, Summing Inputs Feature, Optimized for Battery Life	M	S	2	2.5	5.5	0.2	75	3.3	1	4	✓	✓	—	L	—	—	—	MSOP	AEJ	1.09
TPA0242	Stereo, Headphone Drive, Optimized for Fidelity	S	S	2	4.5	5.5	0.22	67	10	150	3	✓	✓	—	L	—	✓	—	TSSOP	TPA0242	1.50
TPA0243	Mono, Headphone Drive, Summing Inputs Feature, Optimized for Fidelity	M	S	2	2.5	5.5	0.2	75	9	1	4	✓	✓	—	L	—	—	—	MSOP	AEK	1.09
TPA0252	Stereo, Headphone Drive, Gain Memory, Optimized for Battery Life	S	S	2	4.5	5.5	0.3	67	4.5	150	3	✓	✓	—	L	—	—	✓	TSSOP	TPA0252	1.69
<b>TPA6010A4</b>	Stereo, Headphone Drive, Bass Boost, Buffered Docking Station Outputs, Fully Differential Inputs	S	S	2	4.5	5.5	0.5	67	6	60	3	✓	✓	—	L	—	✓	—	TSSOP	TPA6010A4	2.14
TPA6011A4	Stereo, Headphone Drive, Differential Inputs, Fade Mode, Independent Maximum Gain Settings	S	S	2	4	5.5	N/A	70	3.8	1	3	✓	✓	—	L	—	—	✓	TSSOP	TPA6011A4	1.41
TPA6017A2	Stereo, Fully Differential Inputs	S	—	2	4.5	5.5	0.75	77	3	150	3	—	✓	—	L	✓	—	—	TSSOP	TPA6017A2	1.21
TPA2000D1	Mono, Filter-Free, Class-D, Differential Input	M	—	2	2.7	5.5	0.04	77	4	0.05	4	—	✓	—	L	✓	—	—	TSSOP	TPA2000D1	0.99

<sup>1</sup>New products appear in **BOLD RED**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.



Device <sup>1</sup>	Description	Stereo/ Mono Speaker Drive	Stereo/ Mono Head- phone Drive	Output Power (W)	V <sub>CC</sub> (V) (min)	V <sub>DD</sub> (V) (max)	THD+N at 1 kHz (%)	PSRR (dB)	I <sub>Q</sub> Per Ch. (mA) (typ)	I <sub>SD</sub> (μA)	Min Load Impe- dance (Ω)	Input MUX	Depop	Mute	SHDN (Active Low/ High)	Int. Gain	DC Volume Control	Digital Volume Control	Package(s)	Package Symbol- ization	Price <sup>2</sup>
TPA2000D2	Stereo, Filter-Free, Class-D, Differential Input	S	—	2	4.5	5.5	0.5	77	4	1	3	—	✓	—	L	✓	—	—	TSSOP	TPA2000D2	1.34
TPA2000D4	Stereo, Filter-Free, Class-D, Differential Input, Class-AB Headphone Amp with Depop	S	S	2	3.7	5.5	0.3	70	4.5	0.05	4	—	✓	—	L	✓	—	—	TSSOP	TPA2000D4	1.29
<b>TPA6203A1</b>	Mono, Fully Differential Inputs	M	—	1.25	2.5	5.5	0.06	90	1.7	0.01	8	—	✓	—	L	—	—	—	μ*BGA Jr™		0.45
TPA0253	Mono, Headphone Drive, Summing Inputs, Optimized for Battery Life	M	S	1	2.5	5.5	0.2	75	2.7	1	8	—	✓	—	L	—	—	—	MSOP	AEL	0.94
TPA2001D1	Mono, Filter-Free, Class-D, Differential Input	M	—	1	2.7	5.5	0.4	72	4	0.05	8	—	✓	—	L	✓	—	—	TSSOP	TPA2001D1	0.70
TPA2001D2	Stereo, Filter-Free, Class-D, Differential Input	S	—	1	4.5	5.5	0.5	77	4	1	8	—	✓	—	L	✓	—	—	TSSOP	TPA2001D2	1.14
<b>TPA2005D1</b>	Mono, Filter-Free, Class-D, Differential Input, Synchronized Switching Frequency	M	—	1.1	2.5	5.5	0.2	80	4	1	8	—	✓	—	L	—	—	—	μ*BGA Jr		0.49
TPA711	Mono, Earphone Drive	M	M	0.7	2.5	5.5	0.2	85	1.25	7	8	—	✓	—	H	—	—	—	SOIC, MSOP	TPA711 ABB	0.41
TPA721	Mono	M	—	0.7	2.5	5.5	0.2	85	1.25	7	8	—	✓	—	H	—	—	—	SOIC, MSOP	TPA721 ABC	0.41
TPA731	Mono, Differential Inputs, Compatible with LM4871	M	—	0.7	2.5	5.5	0.2	78	1.25	0.0015	8	—	—	—	H	—	—	—	SOIC, MSOP	TPA731 AJC	0.41
TPA741	Mono, Differential Inputs	M	—	0.7	2.5	5.5	0.2	85	1.35	7	8	—	✓	—	H	—	—	—	SOIC, MSOP	TPA741 AJD	0.41
TPA751	Mono, Differential Inputs	M	—	0.7	2.5	5.5	0.2	78	1.25	0.0015	8	—	—	—	L	—	—	—	SOIC, MSOP	TPA751 ATC	0.41
TPA301	Mono, Pin Compatible with LM4864	M	—	0.35	2.5	5.5	0.3	78	0.7	0.15	8	—	—	—	H	—	—	—	SOIC, MSOP	TPA301 AAA	0.29
TPA311	Mono, Earphone Drive	M	M	0.35	2.5	5.5	0.3	78	0.7	7	8	—	✓	—	H	—	—	—	SOIC, MSOP	TPA311 AAB	0.29
TPA321	Mono, Differential Inputs	M	—	0.35	2.5	5.5	0.3	78	0.7	0.15	8	—	—	—	H	—	—	—	SOIC, MSOP	TPA321 AJB	0.29
TPA6110A2	Stereo, Headphone, Pin Compatible with LM4881	—	S	0.15	2.5	5.5	0.03	83	0.75	10	16	—	✓	—	H	—	—	—	MSOP	AIZ	0.39
TPA6111A2	Stereo, Headphone, Pin Compatible with LM4880 and LM4881	—	S	0.15	2.5	5.5	0.03	83	0.75	1	16	—	✓	—	H	—	—	—	SOIC, MSOP	TPA6111A2 AJA	0.29
TPA6112A2	Stereo, Headphone, Differential Inputs	—	S	0.15	2.5	5.5	0.03	83	0.75	10	16	—	✓	—	H	—	—	—	MSOP	APD	0.29
TPA152	Stereo, Headphone	—	S	0.075	4.5	5.5	0.02	81	2.8	—	32	—	✓	✓	—	—	—	—	SOIC	TPA152	0.50
TPA6100A2	Ultra-Low Voltage, Stereo, Headphone	—	S	0.05	1.6	3.6	0.2	72	0.38	0.05	16	—	✓	—	L	—	—	—	SOIC, MSOP	TPA6100A2 AJL	0.33
TPA6101A2	Ultra-Low Voltage, Stereo, Headphone, Fixed Gain (2 dB)	—	S	0.05	1.6	3.6	0.4	72	0.32	0.05	16	—	✓	—	L	—	—	—	SOIC, MSOP	TPA6101A2 AJM	0.33
TPA6102A2	Ultra-Low Voltage, Stereo, Headphone, Fixed Gain (14 dB)	—	S	0.05	1.6	3.6	0.4	72	0.32	0.05	16	—	✓	—	L	—	—	—	SOIC, MSOP	TPA6103A1 AJN	0.33

<sup>1</sup>New products appear in **BOLD RED**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Audio Signal Amplifiers Selection Guide

Device <sup>1</sup>	Description	Channels	Supply Voltage (V)	THD+N (%)	Slew Rate (V/μs)	GBW (MHz)	Package(s)	Price <sup>2</sup>
<b>Operational Amplifiers</b>								
OPAy343	CMOS, Single Supply	1, 2, 4	2.5 to 5.5	0.0007	6	5.5	SOT23, MSOP, TSSOP, SSOP, SOIC	0.66
OPAy353	CMOS, Single Supply, High Speed	1, 2, 4	2.7 to 5.5	0.0006	22	44	SOT23, MSOP, TSSOP, SOIC	1.05
OPAy604	FET-Input	1, 2	±4.5 to ±24	0.0003	25	20	DIP, SOIC	0.91
OPAy134	FET-Input	1, 2, 4	±2.5 to ±18	0.00008	20	8	DIP, SOIC	0.88
OPAy227	Low Noise	1, 2, 4	±2.5 to ±18	0.00005	2.3	8	DIP, SOIC	1.01
OPAy228	Low Noise	1, 2, 4	±2.5 to ±18	0.00005	10	33	DIP, SOIC	1.01
OPAy627	Ultra-High Performance, DiFET	1	±4.5 to ±18	0.00003	55	16	DIP, SOIC, TO-99	9.63
OPAy637	Ultra-High Performance, DiFET, G ≥ 5	1	±4.5 to ±18	0.00003	135	80	DIP, SOIC, TO-99	9.63
<b>OPAy363</b>	1.8 V, High CMR, RRIO, SHDN, SS	1, 2	1.8 to 5.5	—	5	7	SOT23, MSOP, SOIC	0.55
<b>Line Drivers and Receivers</b>								
DRV134	Professional Line Transmitter	1	±4.5 to ±18	0.0005	12	1.5	DIP, SOIC, SOL	1.82
DRV135	Professional Line Transmitter	1	±4.5 to ±18	0.0005	12	1.5	DIP, SOIC, SOL	1.82
INA134	Professional Line Receiver, Low Distortion, G = 1	1	±4 to ±18	0.0005	14	3.1	DIP, SOIC	1.00
INA2134	Dual INA134	2	±4 to ±18	—	14	3.1	DIP, SOIC	1.82
INA137	Professional Line Receiver, G = 0.5 or 2	1	±4 to ±18	0.0005	14	4	DIP, SOIC	0.99
INA2137	Dual INA137	2	±4 to ±18	0.0005	14	4	DIP, SOIC	0.99
<b>Microphone Preamplifiers</b>								
INA163	Low Noise, High Performance	1	±4.5 to ±18	0.0003	15	8	SO-14	2.35
INA166	Low Noise, Fixed Gain, 2000 V/V	1	±4.5 to ±18	—	15	4.5	SO-14	5.66
INA103	High Performance, Low Distortion	1	±9 to ±25	—	15	8	DIP, SOL-16	4.65
INA217	Low Noise	1	±4.5 to ±18	0.004	15	8	DIP, SOIC	2.35

<sup>1</sup>New products appear in **BOLD RED**. *y* indicates: no character = single, 2 = dual, 3 = triple, 4 = quad. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Digitally Programmable Gain Audio Amplifiers Selection Guide

Device	Description	Number of Channels	Dynamic Range (dB)	THD+N at 1kHz (%)	Crosstalk at 1 kHz (%)	Power Supply (V)	Voltage Swing (V <sub>p-p</sub> )	Package(s)	Price <sup>1</sup>
PGA2310	BiCMOS, Stereo Audio Volume Control	2	120	0.0004	-126	±15	27	SO-16, PDIP-16	7.95
PGA2311	CMOS, Stereo Audio Volume Control	2	120	0.0002	-130	±5	7.5	SO-16, PDIP-16	4.95
PGA4311	CMOS, 4-channel Audio Volume Control	4	120	0.0002	-130	±5	7.5	SO-28	8.45

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Digital Amplifiers Power Stage Selection Guide

Device <sup>1</sup>	Description	Ch.	F <sub>S</sub> (kHz) (min)	F <sub>S</sub> (kHz) (max)	Dynamic Range (dB)	Power (WRMS at 6 Ω)	THD+N at 1kHz (%)	Efficiency (%)	Package(s)	Price <sup>2</sup>
TAS5100A	Mono, 30 W, Power Stage	1	32	192	93	30	< 0.08	> 90	HTSSOP-32	3.15
TAS5101	Stereo, 15 W, Power Stage	2	32	192	96	13	< 0.08	> 90	HTSSOP-32	3.44
TAS5110	Mono, 50 W, Power Stage	1	32	192	96	43	< 0.08	> 90	HTSSOP-32	3.19
<b>TAS5182</b>	Stereo, 100 W, Power Stage	2	32	192	101	100	< 0.08	> 90	HTSSOP-56	—


<sup>1</sup>New products appear in **BOLD RED**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Digital Audio PWM Processors Selection Guide

Device	Channels	Sample Frequency (kHz)	Dynamic Range (dB)	THD+N (% of System Performance)	Bits	Package(s)	Price <sup>1</sup>
TAS5026	6	32 to 192	96	< 0.08	16, 20, 24	PQFP-64	7.27
TAS5036	6	32 to 192	100	< 0.08	16, 20, 24	PQFP-80	13.90
TAS5001	2	32 to 96	96	< 0.08	16, 20, 24	PQFP-48	2.53
TAS5010	2	32 to 192	96	< 0.08	16, 20, 24	PQFP-48	3.17
TAS5012	2	32 to 192	102	< 0.08	16, 20, 24	PQFP-48	5.89
TAS5015 <sup>2</sup>	2	32 to 192	110	< 0.01	16, 20, 24	PQFP-48	25.00

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000. <sup>2</sup>Requires equibit license.

# Power Amplifiers and Buffers

 TI power amplifiers solve tough high-voltage and high-current design problems in applications requiring up to 300-V and 15-A output current. Most are internally protected against thermal and current overload and some offer user-defined current limit. The unity-gain buffer amplifier series provides slew rates up to 3600 V/ $\mu$ s and output current to 250 mA.

## Design Considerations

**Power dissipation**—determines the appropriate package type as well as the size of the required heat sink. Always stay within the safe operating range to avoid damage and increase reliability of the power amps. Some power amps are internally protected against overheating and overcurrent. The thermally enhanced PowerPAD™ package provides greater design flexibility and

increased thermal efficiency in a standard size IC package. PowerPAD provides an extremely low thermal resistance path to a ground plane or special heat sink structure.

**Full-power bandwidth**—or large-signal bandwidth, high FPBW is achieved by using power amps with high slew rate.

**Current limit**—be aware of the safe operating area, which defines the relationship between supply voltage and current output. Both power supply and load must be appropriately selected to avoid thermal and current limits.

**Thermal shutdown**—the incorporation of internal thermal sensing and shut-off will automatically shut off the amplifier should the internal temperature reach a specified value.

## Technical Information

### Power Amps

Unlike other designs using a power resistor in series with the output current path, the OPA547, OPA548 and OPA549 power amps sense current internally. This allows the current limit to be adjusted from near 0 A to the upper limit with a control signal or a low-power resistor. This feature is included in the OPA56x series.

### Buffers

The BUF634 can be used inside the feedback loop to increase output current, eliminate thermal feedback and improve capacitive load drive. When connected inside the feedback loop, the offset voltage and other errors are corrected by the feedback of the op amp.

## Power Amplifiers Selection Guide

Device	I <sub>OUT</sub> (A)	V <sub>S</sub> (V)	Bandwidth (MHz)	Slew Rate (V/ $\mu$ s)	I <sub>Q</sub> (mA) (max)	V <sub>OS</sub> (mV) (max)	V <sub>O</sub> Drift ( $\mu$ V/ $^{\circ}$ C) (max)	I <sub>B</sub> (nA) (max)	Package(s)	Price <sup>1</sup>
3581	0.03	64 to 150	5 at G = 1	20	8	3	25	0.02	TO-3	122.68
3583	0.075	$\pm$ 70 to $\pm$ 150	5 at G = 1	30	8.5	3	23	0.02	TO-3	99.57
3584	0.015	$\pm$ 70 to $\pm$ 150	50	150	6.5	3	25	0.02	TO-3	99.57
OPA445/B	0.015	10 to 40	2	15	4.7	5 / 3	10	0.05	T099, DIP8, SO8	2.47
OPA452	0.05	20 to 80	1.8	7.2	5.5	3	5	0.1	T0220-7, DDPak-7	2.40
OPA453	0.05	20 to 80	7.5	23	5.5	3	5	0.1	T0220-7, DDPak-7	2.40
OPA512	15	$\pm$ 10 to $\pm$ 50	4	4	35	3	40	20	TO-3	59.31
OPA541	10	$\pm$ 10 to $\pm$ 40	full power 55 kHz	10	20	1	30	0.05	TO-3, ZIP	10.55
OPA2541	5	$\pm$ 10 to $\pm$ 40	full power 55 kHz	6	50	1	30	0.05	TO-3	39.40
OPA544	2	20 to 70	1.4	8	12	5	10	0.1	T0220-5, DDPak-5	6.68
OPA2544	2	20 to 70	1.4	8	12	5	10	0.1	ZIP11	11.43
OPA547	0.5	8 to 60	1	6	10	5	25	500	T0220-7, DDPak-7	4.14
OPA548	3	8 to 60	1	10	17	10	30	500	T0220-7, DDPak-7	5.52
OPA549	8	8 to 60	0.9	9	26	5	20	500	ZIP11	10.96
OPA551	0.2	8 to 60	3	15	7	3	7	0.1	DIP8, SO8, DDPak-7	1.66
OPA552	0.2	8 to 60	12	24	7	3	7	0.1	DIP8, SO8, DDPak-7	1.66
OPA561	1.2	7 to 16	17	50	50	20	50	0.1	HTSSOP-20	2.50
TLV411x	0.3	2.5 to 6	2.7	1.6	1	3.5	3	0.05	PDIP, MSOP, SOIC	0.65

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

## Buffers Selection Guide

Device	V <sub>S</sub> $\pm$ 15 (V)	V <sub>S</sub> $\pm$ 5 (V)	V <sub>S</sub> 5 (V)	A <sub>CL</sub> Min Stable Gain (V/V)	BW at A <sub>CL</sub> (MHz)	Slew Rate (V/ $\mu$ s)	Settling Time (0.01%) (ns) (typ)	I <sub>Q</sub> (mA) (typ)	THD (F <sub>C</sub> = 1 MHz) (dB) (typ)	Diff Gain (%)	Diff Phase ( $^{\circ}$ )	V <sub>N</sub> at Flatband (nV/ $\sqrt$ Hz) (typ)	V <sub>OS</sub> (mV) (max)	I <sub>B</sub> ( $\mu$ A) (max)	Package(s)	Price <sup>1</sup>
BUF600	—	Yes	—	1	320	3400	—	20	-62	0.5	0.02	5.2	30	3.5	DIP, SOIC	2.62
BUF601	—	Yes	—	1	320	3600	—	20	-60	0.4	0.03	4.8	30	3.5	SOIC	3.63
BUF634	Yes	Yes	Yes	1	180	2000	200	250	—	0.4	0.1	4	100	20	DIP, SOIC, T0220-5, DDPak-5	2.87
OPA633	Yes	Yes	—	1	260	2500	50	100	—	—	0.1	—	15	35	DIP	5.15

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

# Pulse Width Modulation Drivers

Texas Instruments' pulse width modulation (PWM) power drivers are ideal for any application that requires high current at low voltages, such as electro-mechanical devices, thermoelectric coolers or laser diodes. The DRV59x devices feature integrated power transistors, which save considerable circuit board area compared to discrete implementations. The H-bridge output configuration allows for bi-directional current flow from a single power supply. Unlike the operation of linear drivers, PWM operation offers efficiencies as great as 90 percent, resulting in less power wasted as heat and reduced demand on the power supply. The devices in the DRV59x family may be analog or digitally controlled and operate from 0 to 100 percent duty cycle.

## Design Considerations

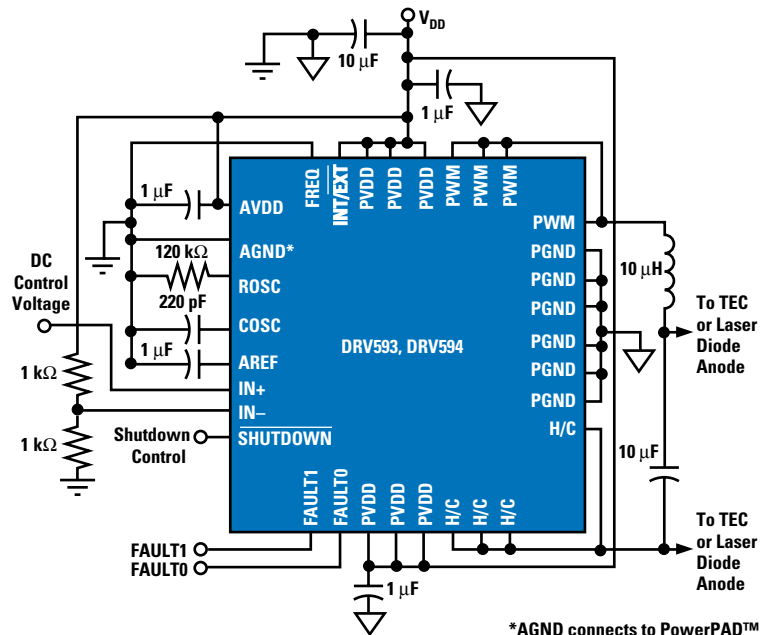
**Supply voltage**—selection begins with the power supply voltages available in the system. TI's family PWM power drivers operate from 2.8 V to 5.5 V.

**Output current and output voltage**—the load to be connected to the power driver will also help determine the proper PWM power driver solution. The maximum output current required by the load should be known. The DRV590 can sink or source up to 1.2 A, while the DRV591, DRV592, DRV593 and DRV594 can each sink or source up to 3 A. The maximum output voltage capability of the driver may be calculated as follows:

$$V_O(\text{max}) = V_S - [I_O(\text{max}) \cdot 2 \cdot R_{DS(ON)}]$$

**Efficiency**—the lower the on-resistance ( $R_{DS(ON)}$ ) of the output power transistors,

DRV593/DRV594 Typical Application Schematic



the greater the efficiency. Typically,  $R_{DS(ON)}$  is specified per transistor. In an H-bridge output configuration, two output transistors are in series with the load. To quickly estimate the efficiency, use the following equation:

$$\text{Efficiency} = R_L / [R_L + (2 \cdot R_{DS(ON)})]$$

**Analog or digital control**—the DRV590, DRV591, DRV593 and DRV594 each accept a DC voltage input signal, either from an analog control loop (i.e. PID controller) or from a DAC. The DRV592 accepts a PWM input signal up to 1 MHz, which may be generated by a microcontroller, FPGA or DSP.

**Output filter**—in some applications, a low-pass filter is placed between each output of the PWM driver and the load to remove

the switching frequency components. A second-order filter consisting of an inductor and capacitor is commonly used, with the cut-off frequency of the filter typically chosen to be at least an order of magnitude lower than the switching frequency. For example, for the DRV593 (shown above), the switching frequency is 500 kHz and the cut-off frequency is chosen to be 15.9 kHz. The component values are calculated using the following formula:

$$F_C = 1 / [2 \cdot \pi \cdot (\sqrt{L \cdot C})]$$

The inductor value is typically chosen to be as large as possible, and is then used to calculate the required capacitor value for the desired cut-off frequency.

## PWM Power Drivers Selection Guide

Device	Output Current (A) (typ)	Supply Voltage (V)	Switching Frequency (kHz)	$R_{DS(ON)}$ ( $\Omega$ )	CMV Range (V)	$I_Q$ (mA)	Fault indicator for thermal, over-current and under-voltage conditions	Package(s)	Price <sup>1</sup>
DRV590	1.2	2.8 to 5.5	500	0.4	1.2 to 3.8	4	—	PowerPAD™, SOIC, TSSOP, 4 x 4 mm MicroStar Junior™	6.96
DRV591	3	2.8 to 5.5	100/500	0.065	1.2 to 3.8	7	✓	9 x 9 mm PowerPAD™ Quad Flatpack	12.34
DRV592	3	2.8 to 5.5	1000	0.065	—	7	✓	9 x 9 mm PowerPAD Quad Flatpack	11.90
DRV593	3	2.8 to 5.5	100/500	0.065	1.2 to 3.8	7	✓	9 x 9 mm PowerPAD Quad Flatpack	11.90
DRV594	3	2.8 to 5.5	100/500	0.065	1.2 to 3.8	7	✓	9 x 9 mm PowerPAD Quad Flatpack	11.90

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

# 4-20 mA Transmitters

The 4-20 mA transmitter provides a versatile instrumentation amplifier (IA) input with a current-loop output, allowing analog signals to be sent over long distances without loss of accuracy. Many of these devices also include scaling, offsetting, sensor excitation and linearization circuitry.

## Design Solutions

XTR101, XTR115 and XTR116 provide general-purpose 2-wire (loop powered) conversion of signal input voltages or currents to the 4-20 mA standard output. They contain reference voltage or current sources for ease of scaling or sensor excitation where hardware linearization is not needed.

The XTR110 is a 3-wire 4-20 mA converter from 0 V to 5 V or 0 V to 10 V voltage inputs. The RCV420 is an accurate 4-20 mA input to 0 V to 5 V output receiver that introduces only a 1.5 V drop in the 4-20 mA loop.

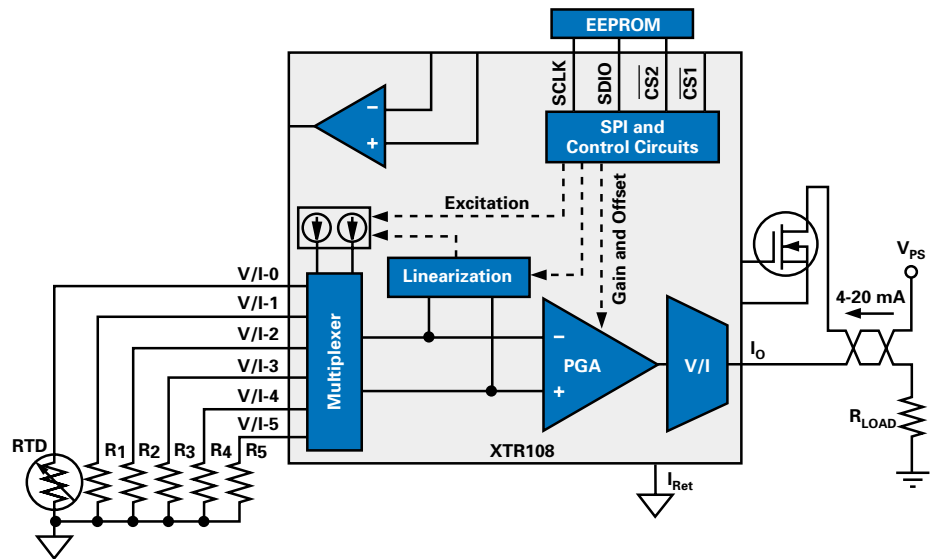
XTR105, XTR112 and XTR114 provide current source sensor excitation and hardware linearization for 100  $\Omega$ , 1 k $\Omega$  and 10 k $\Omega$  RTDs.

The XTR106 provides an accurate 2.5 V or 5 V sensor excitation voltage for conditioning bridge transducers and includes hardware linearization.

The XTR108 provides a digitally controlled analog signal path for RTD signal conditioning. The XTR108 allows for digital

calibration of sensor and transmitter errors via a standard digital serial interface, eliminating expensive potentiometers or circuit value changes. Calibration settings can be stored in an inexpensive EEPROM for easy retrieval during routine operation.

XTR108 Digitally Programmable Analog Sensor Conditioning



## 4-20 mA Transmitters and Receiver Selection Guide

Device	Description	Sensor Excitation	Loop Voltage (V)	Full-Scale Input Range	Output Range (mA)	Additional Power Available (V at mA)	Package(s)	Price <sup>1</sup>
<b>2-Wire General Purpose</b>								
XTR101	IA with Current Excitation	Two 1 mA	11.6 to 40	5 mV to 1 V	4-20	—	DIP-14, SOIC-16	7.34
XTR115	$I_{IN}$ to $I_{OUT}$ Converter, External Resistor Scales $V_{IN}$ to $I_{IN}$	$V_{REF} = 2.5$ V	7.5 to 36	40 $\mu$ A to 200 $\mu$ A	4-20	—	SOIC-8	0.95
XTR116	$I_{IN}$ to $I_{OUT}$ Converter, External Resistor Scales $V_{IN}$ to $I_{IN}$	$V_{REF} = 4.096$ V	7.5 to 36	40 $\mu$ A to 200 $\mu$ A	4-20	—	SOIC-8	0.95
<b>3-Wire General Purpose</b>								
XTR110	Selectable Input/Output Ranges	$V_{REF} = 10$ V	13.5 to 40	0 V to 5 V, 0 V to 10 V	4-20, 0-20, 5-25	—	DIP-16	6.35
<b>4-20mA Current Loop Receiver</b>								
RCV420	4-20 mA Input, 0-v to 5-V Output, 1.5-V Loop Drop	$V_{REF} = 10$ V	+11.5/-5 to $\pm$ 18	4-20 mA	0 V to 5 V	—	DIP-16	3.34
<b>2-Wire RTD Conditioner with Linearization</b>								
XTR105	100- $\Omega$ RTD Conditioner	Two 800 $\mu$ A	7.5 to 36	5 mV to 1 V	4-20	5.1 at 1	DIP-14, SOIC-14	3.75
XTR112	High-Resistance RTD Conditioner	Two 250 $\mu$ A	7.5 to 36	5 mV to 1 V	4-20	5.1 at 1	DIP-14, SOIC-14	3.75
XTR114	High-Resistance RTD Conditioner	Two 100 $\mu$ A	7.5 to 36	5 mV to 1 V	4-20	5.1 at 1	DIP-14, SOIC-14	3.75
<b>2-Wire Bridge Sensor Conditioner with Linearization</b>								
XTR106	Bridge Conditioner	5 V and 2.5 V	7.5 to 36	5 mV to 1 V	4-20	5.1 at 1	DIP-14, SOIC-14	3.75
<b>2-Wire RTD Conditioner with Digital Calibration for Linearization, Span and Offset</b>								
XTR108	100- $\Omega$ to 1-k $\Omega$ RTD Conditioner, 6-Channel Input Mux, Extra Op Amp Can Convert to Voltage Sensor Excitation, Calibration Stored in External EEPROM	Two 500 $\mu$ A	7.5 to 24	5 mV to 320 mV	4-20	5.1 at 2.1	SSOP-24	3.21

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

# Logarithmic Amplifiers

The logarithmic amplifier is a versatile integrated circuit that computes the logarithm of an input current relative to a reference current or the log of the ratio of two input currents. Logarithmic amplifiers can compress an extremely wide input dynamic range (up to 7½ decades) into an easily measured output voltage. Accurate matched bipolar transistors provide excellent logarithmic conformity over a wide input current range. On-chip compensation achieves accurate scaling over a wide operating temperature range.

The LOG101, LOG102 and LOG104 are designed for optical networking, photodiode signal compression, analog signal compression and logarithmic computation for instrumentation. Some log amps, such as the LOG102, feature additional uncommitted op amps for use in a variety of functions including gain scaling, inverting, filtering, offsetting and level comparison to detect loss of signal.

The new **LOG2112** is a dual version of the LOG112 and includes 2 log amps, 2 output amps and a single shared internal voltage reference.

## Design Considerations

**Output scaling**—amplifier output is either 0.5 V or 1.0 V per decade and is the equivalent to the gain setting in a voltage input amp.

**Quiescent current**—lowest in LOG101 and LOG104.

**Conformity error**—measure with 1 nA to 1 mA converted to 5 V. 16-bits of dynamic range are achievable.

**Auxiliary op amps**—some log amps have additional uncommitted op amps that can be used to offset and scale the output signal to suit application requirements.

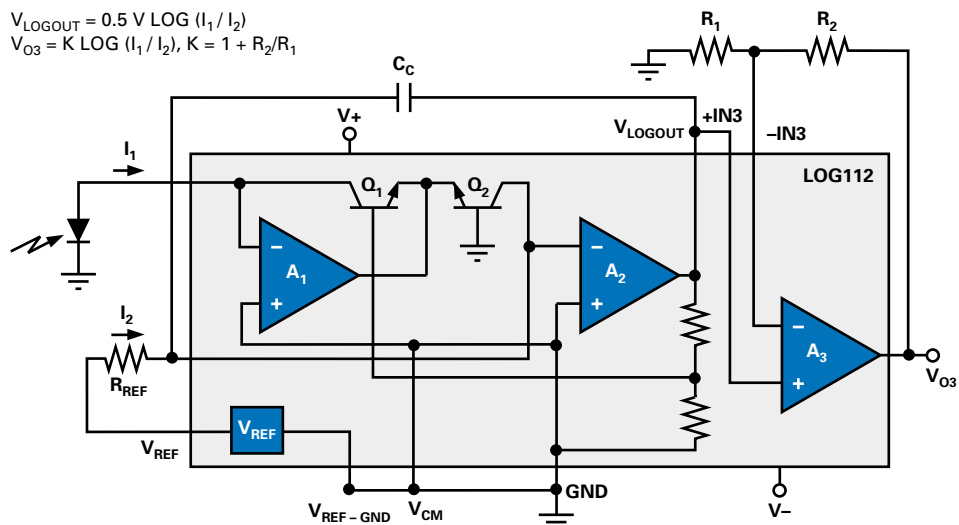
## Technical Information

Log amplifiers provide a very wide dynamic range (140 dB+), extremely good DC accuracy and excellent performance over the full temperature range.

LOG112 Block Diagram

$$V_{\text{LOGOUT}} = 0.5 \text{ V LOG} (I_1 / I_2)$$

$$V_{\text{O3}} = K \text{ LOG} (I_1 / I_2), K = 1 + R_2/R_1$$



NOTE: Internal metal resistors are used to compensate gain change over temperature.

## Logarithmic Amplifiers Selection Guide

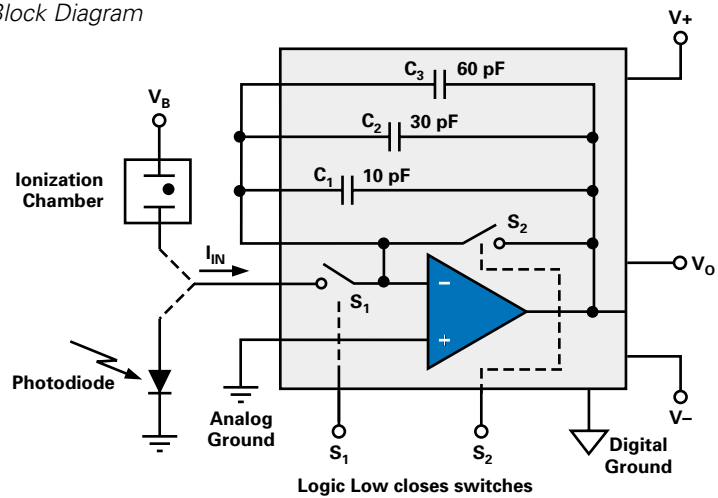
Device <sup>1</sup>	Scale Factor (V/decade)	Input Current Range (nA) (min)	Input Current Range (mA) (max)	Conformity Error (Initial 5 decades) (%) (max)	Conformity Error (Initial 5 decades) (%/°C) (typ/temp)	Offset Voltage (Input Amplifiers) (mV) (max)	V <sub>S</sub> (V) (min)	V <sub>S</sub> (V) (max)	I <sub>Q</sub> Per Ch. (mA) (max)	Reference Type	Auxiliary Op Amps	Package(s)	Price <sup>2</sup>
LOG100	1	1	1	0.1	0.002	5	±12	±18	9	External	—	Hermetic Ceramic DIP-14	82.99
LOG101	1	0.1	3.5	0.2	0.0001	1.5	±4.5	±18	1.5	External	—	SO-8	15.65
LOG102	1	1	1	0.3	0.0002	1.5	±4.5	±18	2	External	2	SO-14	18.65
LOG104	0.5	0.1	3.5	0.2	0.0001	1.5	±4.5	±18	1.5	External	—	SO-8	15.65
LOG112	0.5	0.1	3.5	0.2	0.00001	1.5	±4.5	±18	1.75	2.5 V Internal	1	SO-14	18.65
<b>LOG2112<sup>3</sup></b>	0.5	0.1	3.5	0.2	0.00001	1.5	±4.5	±18	1.75	2.5 V Internal	1	SO-16	22.30

<sup>1</sup>New products appear in **BOLD RED**. <sup>2</sup>Suggested resale price in U.S. dollars in quantities of 1,000. <sup>3</sup>Dual LOG112.



**▶** Integrating amplifiers provide a precision, lower noise alternative to conventional transimpedance op amp circuits which require a very high value feedback resistor. Designed to measure input currents over an extremely wide dynamic range, integrating amplifiers incorporate a FET op amp, integrating capacitors, and low-leakage FET switches. Integrating low-level input current for a user-defined period, the resulting voltage is stored on the integrating capacitor, held for accurate measurement and then reset. Input leakage of the IVC102 is just 750 fA. It can measure bipolar input currents.

IVC102 Block Diagram



The ACF2101 two-channel integrator offers extremely low bias current, low noise, an extremely wide dynamic range and excellent channel isolation. Included on each of the two integrators are precision 100-pF integration capacitors, hold and reset switches and output multiplexers. As a complete circuit on a chip, leakage current and noise pickup errors are eliminated. An output capacitor can be used in addition to, or instead of the internal capacitor depending on design requirements.

## Design Considerations

**Supply voltage**—while single-supply operation is feasible, bipolar supply operation is most common and will offer the best performance in terms of precision and dynamic range.

**Number of channels**—IVC102 offers a single integrator, while the ACF2101 is a dual.

**Integration direction**—either into or out of the device. IVC102 is a bipolar input current integrator and will integrate both positive and negative signals. ACF2101 is a unipolar current integrator, with the output voltage integrating negatively.

**Input bias (leakage) current**—often sets a lower limit to the minimum detectable signal input current. Leakage can be subtracted from measurements to achieve extremely low-level current detection (<10 fA). Circuit board leakage currents can also degrade the minimum detectable signal.

**Sampling rate and dynamic range**—the switched integrator is a sampled system controlled by the sampling frequency ( $f_s$ ), which is usually dominated by the integration time. Input signals above the

Nyquist frequency ( $f_s/2$ ) create errors by being aliased into the sampling frequency bandwidth.

## Technical Information

Although these devices use relatively slow op amps, they may be used to measure very fast current pulses. Photodiode or sensor capacitance can store pulse charge temporarily, the charge is then slowly integrated during the next cycle.

See OPT101 data sheet for monolithic photodiode and transimpedance amplifier.

## Integrating Amplifiers Selection Guide

Device	Description	Input Bias Current (fA)	Switching Time ( $\mu$ s)	Useful Sampling Rate (kHz)	Input Current Range ( $\mu$ A)	Package(s)	Price <sup>1</sup>
IVC102	Precision, Low Noise, Bipolar Input Current	100	100	10	0.01 to 100	SO-14	4.31
ACF2101	Dual, Unipolar	100	200	10	0.01 to 100	SO-24	14.82
<b>Monolithic Photodiode and Transimpedance Amplifier</b>							
OPT101	Monolithic Photodiode with Built-in Transimpedance Amp	165	—	—	—	DIP, SIP	2.58

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

# Isolation Amplifiers

Isolation amplifiers transfer an analog signal across a galvanically isolated barrier. Similar to an optically isolated digital coupler, they generally require an isolated supply to power both sides of the amplifier. Some isolation amplifiers provide an internal isolated power source for the input-side of the amplifier.

Isolation amplifiers can be used to:

- Amplify and measure low-level signals in the presence of high common-mode voltages
- Break ground loops and/or eliminate source ground connections
- Provide an interface between a patient and medical monitoring equipment
- Provide isolation protection to electronic instruments and equipment

## Design Considerations

**Isolation voltage rating**—the maximum voltage that can be applied between the input and output sides of the amplifier. This can range up to thousands of volts. AC and DC ratings may differ and application requirements may dictate safety factors or special industry standards.

**Internal power**—an on-chip DC/DC converter powers the amplifier's front-end on

the ISO103, ISO107 and ISO113. All others require an external isolated power source.

### Isolation type

- *Optically-coupled*—provide continuous signal transfer using two accurately matched couplers—one for the forward signal path and one for feedback. This assures excellent accuracy.
- *Capacitive-coupled*—transmit a differential pulse-coded representation of the analog input across two matched capacitors. The output section reconstructs the analog signal.
- *Transformer-coupled*—use similar modulation techniques to transmit an AC-modulated signal across the magnetic barrier.

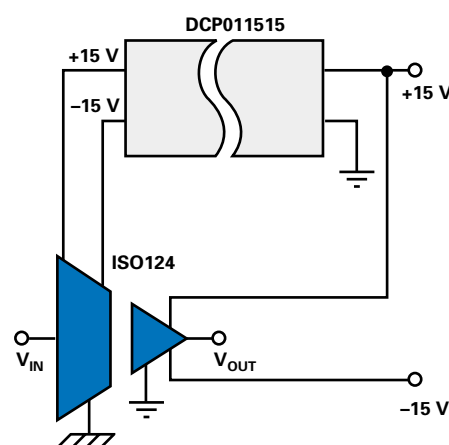
**Leakage current**—cap isolation amps, such as the ISO120/124 series, generally have 0.5- $\mu$ Arms maximum leakage current at 240 V/60 Hz. Opto-isolation amps have leakage current in the 2- $\mu$ Arms maximum range.

## Technical Information

Isolation amps with internal DC/DC converters provide signal and power across an isolation barrier, with additional power available for driving additional circuitry.

Wide barrier pin spacing and internal insulation allow for high isolation voltage ratings. Reliability is assured by 100 percent barrier breakdown testing that conforms to UL1244 test methods. Low barrier capacitance minimizes AC leakage currents. The ISO103's high continuous-voltage rating means that the circuit can tolerate isolation voltages to 1500 Vrms. Its 130-dB isolation-mode rejection at 60 Hz is high enough to limit the interference of a 1500 Vrms fault to 0.5 mVrms.

ISO124 Interface to DC/DC Converter



## Isolation Amplifiers Selection Guide

Device	Description	Isolation Voltage Cont Peak (DC) (V)	Isolation Voltage Pulse/Test Peak (V)	Isolation Mode Rejection DC (dB) (typ)	Gain Nonlinearity (%) (max)	Input Offset Voltage Drift ( $\pm\mu$ V/ $^{\circ}$ C) (max)	Small-Signal Bandwidth (kHz) (typ)	Package(s)	Price <sup>1</sup>
3650	Opto Coupled	2000	5000	140	0.05	—	15	Hybrid DIP-32	64.43
3656	Transformer Isolation	3500	8000	125	0.05	—	30	ISO Omni-20	101.92
ISO100	Low Drift, Wide Bandwidth, Opto	750	2500	146	0.07	2	60	DIP-18	58.33
ISO102	Capacitor Coupled	1500	4000	120	0.012	250	70	DIP-24	51.57
ISO103	Capacitor Isolation, Internal DC/DC	2121	5657	130	0.025	—	20	—	77.24
ISO106	Capacitor Isolation	4950	8000	130	0.025	—	70	—	61.18
ISO107	Internal DC/DC Converter	3500	8000	100	0.025	—	20	—	131.20
ISO113	Internal DC/DC Converter	2121	5657	130	0.02	—	20	—	95.88
ISO120	1500-Vrms Isolation, Buffer	2121	2500	160	0.01	150	60	DIP-24	27.50
ISO121	3500-Vrms Isolation, Buffer	4950	5600	—	0.01	—	60	CERDIP-16	36.05
ISO122	1500-Vrms Isolation, Buffer	2121	2400	160	0.02	200	50	DIP-16, SOIC-28	9.36
ISO124	1500-Vrms Isolation, Buffer	2121	2400	140	0.01	—	50	DIP-16, SOIC-28	6.95
<b>Digital Couplers</b>									
ISO150	Dual, Bi-Directional Digital Coupler	1500	2400	—	—	—	—	DIP-12, SO-12	7.47
ISO422	Differential Bus Transceiver	—	—	—	—	—	—	DIP-16	6.07

<sup>1</sup>Suggested resale price in U.S. dollars in quantities of 1,000.

# Technology Primer and Evaluation Modules

## Technology Primer

Understanding of the relative advantages of the basic semiconductor technologies will help in selecting the proper device for a specific application.

**CMOS amps**—when low voltage and/or low power consumption, an excellent speed/power ratio, rail-to-rail performance, low cost and small packaging are primary design considerations, choose a CMOS amp. TI has the world's most complete portfolio of high-performance, low-power CMOS amps in a variety of micropackages.

**High-Speed Bipolar Amps**—when the highest speed at the lowest power is required, bipolar technology delivers the best performance. Extremely good power gain gives very high output power and full

power bandwidths on the lowest quiescent power. Higher voltage requirements are also only satisfied in bipolar technologies.

**Precision Bipolar Amps**—excel in limiting errors relating to offset voltage. These include low offset voltage and temperature drift, high open-loop gain and common-mode rejection. Precision bipolar op amps are used extensively in applications where the source impedance is low, such as a thermocouple amplifier, where voltage errors, offset voltage and drift, are crucial to accuracy.

**Low  $I_B$  FET Amps**—when input impedance is very high, FET-input amps provide better overall precision than bipolar-input amps. Using a bipolar amp in applications with high source impedance (e.g. 500-M $\Omega$




pH probe), the offset, drift and noise produced by bias currents flowing through the source would render the circuit virtually useless. When low current errors are required, FET amps provide extremely low input bias current, low offset current and high input impedance.

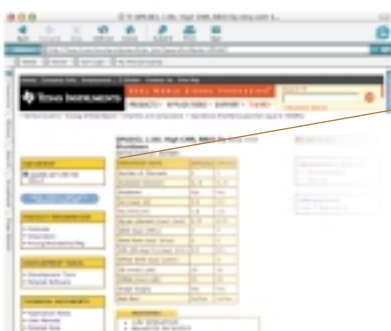
**Dielectrically Isolated FET (DiFET) Amps**—DiFET processing enables the design of extremely low input leakage amplifiers by eliminating the substrate junction diode present in junction isolated processes. This technique yields very high precision, low noise op amps. DiFET processes also minimize parasitic capacitance and output transistor saturation effects, resulting in improved bandwidth and wider output swing.

## Evaluation Modules

To ease and speed the design process, TI offers evaluation modules (EVMs) for many amplifiers and other analog products. EVMs contain an evaluation board, data sheet and user's guide.

To find EVMs, visit [amplifier.ti.com/evm](http://amplifier.ti.com/evm) (right) or the Development Tools section of any individual product folder (below).

<a href="http://amplifier.ti.com/evm">amplifier.ti.com/evm</a>			
	High-Speed Operational Amplifiers	Operational Amplifiers	Audio Power Amplifiers
<b>Hardware Tools</b>			
Development Boards/EVMs	✓ Fully-Populated Ready to Use 	✓ Universal Amplifier Boards 	✓ Fully-Populated Ready to Use 



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- Pricing/Availability/Pkg

**DEVELOPMENT TOOLS**

- **Development Tools**
- Related Software

**TECHNICAL DOCUMENTS**

- Application Notes
- User Manuals
- Related Docs
- Block Diagrams
- Models (SPICE)

Every high speed and audio power amplifier has a fully populated, ready-to-use EVM available. Populated evaluation boards are also available for selected other TI amplifiers. Please see the individual device product folder (left) or contact your local TI sales office for additional choices and availability.

Universal op amp EVMs are unpopulated printed circuit boards that eliminate the need for dual in-line samples in the evaluation of TI amplifiers. These feature:

- Various packages and shutdown
- Ability to evaluate single, dual, or quad amps on several eval spaces per board
- Detachable circuit board development areas for improved portability
- User's manuals with complete board schematic, board layout and numerous standard example circuits
- Product-level Macro Models, designed for use with SPICE, allow efficient simulation of complex circuits without having to use transistor-level models. Download individual models at [amplifier.ti.com/spice](http://amplifier.ti.com/spice)

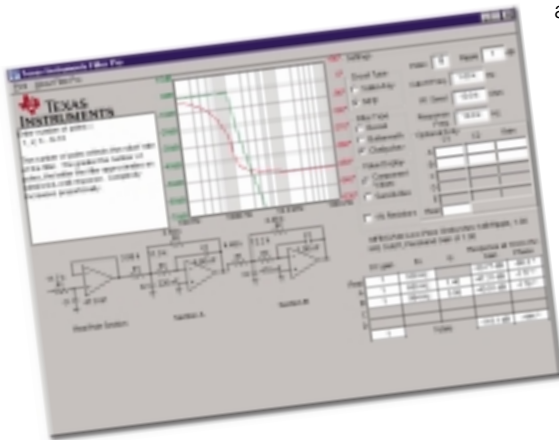
To order your universal op amp EVMs, contact the nearest Product Information Center (PIC) listed on page 39.

# Application Reports

To access any of the following application reports, type the URL [www-s.ti.com/sc/techlit/litnumber](http://www-s.ti.com/sc/techlit/litnumber) and replace litnumber with the number in the Lit Number column. For a complete listing of TI's amplifier application reports visit [amplifier.ti.com/appreports](http://amplifier.ti.com/appreports).

Title	Lit Number
<b>Amplifier Basics</b>	
The Op Amp's Place in the World	SLOA073
Review of Circuit Theory	SLOA074
Development of Ideal Op Amp Equations	SLOA075
Feedback and Stability Theory	SLOA077
Development of the Non-Ideal Op Amp Equations	SLOA078
Understanding Op Amp Parameters	SLOA083
Sine Wave Oscillator	SLOA060
Understanding Basic Analog - Active Devices (Rev. A)	SLOA026
Understanding Basic Analog - Circuit Equations (Rev. A)	SLOA025
Understanding Basic Analog Passive Devices	SLOA027
Understanding Operational Amplifier Specifications	SLOA011
<b>Operational Amplifier Applications</b>	
Use of Rail-to-Rail Operational Amplifiers (Rev. A)	SLOA039
Wireless Communication Signal Conditioning for IF Sampling	SLOA085
Op Amp Noise Theory and Applications	SLOA082
Handbook of Operational Amplifier Applications (Rev. A)	SBOA092
A Single Supply Op Amp Circuit Collection	SLOA058
Handbook of Operational Amplifier Active RC Networks (Rev. A)	SBOA093
Single-Supply Circuit Collection	SLOA091
Conditioning a Switch-mode Power Supply Current Signal	SLOA044
Using TI Op Amps	
Video Designs Using High-Speed Amplifiers	SLOA057
Video Operational Amplifier	SBOA069
Composite Op Amp Gives You The Best of Both Worlds	SBOA002
Ultra High-Speed ICs	SBOA070
<b>Current Feedback Amps</b>	
Current Feedback Amps: Review, Stability Analysis, and Applications	SBOA081
Current Feedback Op Amp Analysis	SLOA080
Voltage Feedback vs. Current Feedback Op Amps	SLVA051
The Current-Feedback Op Amp: A High-Speed Building Block	SBOA076
Current Feedback Amplifier Analysis And Compensation	SLOA021A
A Current Feedback Op-Amp Circuit Collection	SLOA066
<b>Fully Differential Amps</b>	
A Differential Operational Amplifier Circuit Collection	SLOA064
Fully-Differential Amplifiers (Rev. D)	SLOA054
Differential Op Amp Single-Supply Design Techniques	SLOA072
Fully-Differential OP Amps Made Easy	SLOA099
<b>Data Converter Interface</b>	
Instrumentation: Sensors to A/D Converters	SLOA084
Interfacing D/A Converters to Loads	SLOA086
Amplifiers and Bits: An Introduction to Selecting Amplifiers for Data Converters (Rev. B)	SLOA035
Selecting the Right Buffer Operational Amplifier for an ADC	SLOA050
Buffer Op Amp to ADC Circuit Collection	SLOA098
<b>Audio</b>	
Complete Audio Amplifier with Volume, Balance, and Treble Controls	SBOA082
Audio Power Amplifier Solutions for New Wireless Phones	SLOA053
Guidelines for Measuring Audio Power Amplifier Performance	SLOA068
<b>4-20 mA Transmitter</b>	
IC Building Blocks Form Complete Isolated 4-20mA Current-Loop	SBOA017
Single Supply 4-20mA Current Loop Receiver	SBOA023
Use Low-Impedance Bridges on 4-20mA Current Loop	SBOA025

Title	Lit Number
<b>Instrumentation</b>	
Precision Absolute Value Circuits	SBOA068
Programmable-Gain Instrumentation Amplifiers	SBOA024
Signal Conditioning Wheatstone Resistive Bridge Sensors	SLOA034
Instrumentation: Sensors to A/D Converters	SLOA084
AC Coupling Instrumentation and Difference Amplifiers	SBOA003
<b>Power Amps and Buffers</b>	
Combining an Amplifier with the BUF634	SBOA065
Buffer Op Amp to ADC Circuit Collection	SLOA098
<b>Pulse Width Modulation</b>	
PWM Power Driver Modulation Schemes	SLOA092
<b>Transimpedance</b>	
Comparison of Noise Performance of FET Transimpedance Amp/Switched Integrator	SBOA034
Implementation and Applications of Current Sources and Current Receivers	SBOA046
Photodiode Monitoring with Op Amps	SBOA035
Compensate Transimpedance Amplifiers Intuitively	SBOA055
Designing Photodiode Amplifier Circuits with OPA128	SBOA061
<b>Isolation</b>	
Isolation Amps Hike Accuracy and Reliability	SBOA064
Simple Output Filter Eliminates ISO Amp Output Ripple And Keeps Full Bandwidth	SBOA012
Single-Supply Operation of Isolation Amplifiers	SBOA004
<b>Analysis and Design Techniques</b>	
Noise Analysis In Operational Amplifier Circuits	SLVA043A
Current Feedback Amps: Review, Stability Analysis, and Applications	SBOA081
Burr-Brown SPICE Based Macromodels	SBFA009
Using Texas Instruments SPICE Models in PSPICE	SLOA070
Single-Supply Operation of Operational Amplifiers	SBOA059
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Noise Analysis for High Speed Op Amps	SBOA066
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FilterPro MFB and Sallen-Key Low-Pass Filter Design Program	SBFA001A
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More Filter Design on a Budget	SLOA096
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High-Speed Operational Amplifier Layout Made Easy	SLOA046
Effect of Parasitic Capacitance in Op Amp Circuits (Rev. A)	SLOA013
PowerPAD Thermally Enhanced Package Application Report	SLMA002



and capacitors. This program supports Bessel, Butterworth and Chebychev filter types and can be used to design filters from 1 to 10 poles. The capacitor values in each stage can be either selected by the computer or entered by the designer. An "always on" prompt window provides context-sensitive help information to the user. The response of the filter is displayed on a graph, showing gain and phase over frequency.

UAF42 Universal Active Filter IC. This state-variable filter provides low-pass, high-pass and band-pass outputs. Notch filters can also be designed.

EGAFPRES and EGAFXRES are DOS screen dump utilities that can print response plots on HP Laserjet and Epson printers, respectively.

Both programs can be used without documentation but you will eventually need the Application Bulletins for circuit details.

Visit [amplifier.ti.com/filterpro](http://amplifier.ti.com/filterpro) for the free download today.

FilterPro™ MFB and Sallen-Key Design Program is a Windows application that designs Multiple-Feedback and Sallen-Key low-pass filters using op amps, resistors

FilterPro MFB and Sallen-Key Program will install on Win9X and WinNT systems.

FILTER42 is a DOS program that designs a wide variety of filters using Burr-Brown's

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EVMs are available for a wide variety of products.

They are complete with fully-assembled board, data sheet and user's guide. Some may include app notes, software, cables and connectors. Check the product folders for availability.

Need samples fast? Order these online from the product folder, or by phone at **1-800-477-8924** (in North America). See page 39 for contact information for other regions. Samples shipped within 24 hours of receiving the order (except in China).

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