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HIGH PERFORMANCE EPP ETHERNET ADAPTER USING THE PPC34C60 PPIC AND LAN91C92 SCECR

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NOTE: This application note describes a paper design which has not been confirmed by a hardware implementation. This application note should be used to convey the recommended techniques for using the PPC34C60.

DESIGN OVERVIEW:

The design described here showcases the high integration and simplicity of design with the LAN91C92 Single Chip Ethernet Controller and the PPC34C60 ECP/EPP Multi-Mode Parallel Port Peripheral Chip. Both of these 100-pin PQFP ICs are mated to provide a very high performance Ethernet 10Base-T adapter for the parallel port for use with laptops, embedded PCs, or temporary PC-network connections.

The PPC34C60 PPIC regenerates standard ISA bus signals from the ECP/EPP data stream. This part also supports daisy chaining up to 8 EPP devices and one standard parallel port device (such as a printer) by adding J2 (See schematic.) The PPIC reassembles 4 and 8 bit EPP words into 8 and 16-bit wide word transfers to the ISA bus for transfer rates **15 to 80 *times*** that of a standard parallel port interface. The PPIC also supports DMA transfers, but this is not required for the 91C92's PIO interface.

The LAN91C92 SCECR contains 4.5K of buffer RAM, and a unique memory management unit which eliminates much of the overhead that would otherwise need to be handled by the host over the EPP interface. Configuration and Ethernet ID information is stored in a 4-pin serial EEPROM. The seven programmable outputs of the PPIC allow full software configuration of the Ethernet controller. Two of these outputs are used for power management functions.

The software drivers required for this design are identical to the LAN9000 series drivers required for ISA designs. The only modification required is rerouting of direct I/O through EPP BIOS calls instead. Ethernet interrupts will also be serviced through INT5 or 7, rather than INT10 or 11.

DESIGN FEATURES:

- Very simple, compact, and inexpensive design. Two 100-pin PQFPs, 3 crystals, a 10Base-T SMT isolation transformer, a battery (or adapter), and 3 connectors are all that is required for a fully functional system.

- PPIC directly drives piezo buzzer for low battery detection and EPP inactivity. A 22k resistor on pin 35 forms a simple voltage divider with the internal 100K internal pullup to signal a low battery when VCC drops to about 4V.

- EPP inactivity detection with WATCHDOG timer enabled (JP1). This allows the user to be signaled if the adapter is unplugged and put away with the power on.

- PPIC nS0 is used for power management on the 91C92. The Ethernet controller will remain in Standby Mode until the driver software is run to enable the adapter.

- PPIC nS1 is used as an indicator that the PPIC has been initialized properly by the driver software.

- PPIC nS2 is used to control the SCECR EEPROM interface enable.

- PPIC nS3 is used to emulate the Hi-Byte Enable of the 16-bit ISA interface.

- The serial EEPROM is enabled by grounding ENEEP, and IOS0-2 are preset to '000' for software programming by the host of partition 0.

- A Pulse Engineering PE-65486A 10Base-T interface transformer is used with integrated predistortion resistors for increased integration. An alternate transformer could be used for lower cost.

- Alternate AUI interface easily implemented with pins 78-85. 10Base-2/Thin-Ethernet can be added with minimal external circuitry and a coax transceiver chip such as the LAN83B692 .

- Link Integrity, TX and RX Activity LED's are directly driven by the LAN91C92.