DATA SHEET

SILICONDRIVE 1.8" DRIVE

SSD-HXXX(I)-3650

OVERVIEW

SiliconDrive combines all the high performance, high reliability, and multiyear lifecycle benefits of the standard SiliconDrive with a comprehensive suite of patented and patent-pending technologies that provide multiple security options to safeguard application data and software IP in embedded systems.

Applications requiring advanced levels of security such as data recorders, wearable and field computers, medical monitoring and diagnostic equipment, POS systems, and voting machines are able to activate security options to protect application data and software IP from theft, falling into the wrong hands from deployments in high-risk areas, corruption, and accidental or malicious overwrites.

PowerArmor prevents data corruption and loss from power disturbances by integrating patented technology into every SiliconDrive.

SiSMART acts as an early warning system to eliminate unscheduled downtime by constantly monitoring and reporting the exact amount of remaining storage system useful life.

SiSecure is a comprehensive suite of user-selectable security technologies that solves the critical need for robust storage security for embedded systems applications that have a small footprint and low-power requirement.

SISECURE

PowerArmor	Eliminates drive corruption.
SiZone	Data zones with different security parameters.
SiKey	Ties SiliconDrive to a specific host and/or software IP.
SiProtect	Protection software for password-required, read/write, or read-only access.
SiSweep	Ultra-fast data erasure.
SiPurge	Non-recoverable data erasure.

FEATURES

- RoHS 6 of 6 compliant
- Integrated PowerArmor, SiSMART, and SiSecure technologies
- Capacity range: 32MB to 16GB
- Supports both 8-bit and 16-bit data register transfers
- Supports 5V interface
- Data reliability <1 error in 10^{14} bits read
- MTBF >4,000,000 hours
- ATA-3 compliant
- Industry Hitachi 1.8" Drive form factor
- Supports PIO modes 0-4 and DMA modes 0-2

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REVISION HISTORY

Document No.	Release Date	Changes
3650H-02DSR	June 17, 2008	**Updated:** • "Overview." • "SiliconDrive Technology" to "SiSecure."
3650H-01DSR	May 25, 2008	**Updated:** • "Overview." • *SiliconDrive Secure* to *SiSecure*. • SiProtect information.
SSDS00-3650H-R	November 8, 2007	Initial release.

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PHYSICAL SPECIFICATIONS

The SiliconDrive 1.8" Drive products are offered in an industry-standard 1.8" Drive form factor. See "Part Numbering" on page 63 for details regarding 1.8" Drive capacities.

PHYSICAL DIMENSIONS

This section provides diagrams that describe the physical dimensions for the 1.8" Drive.

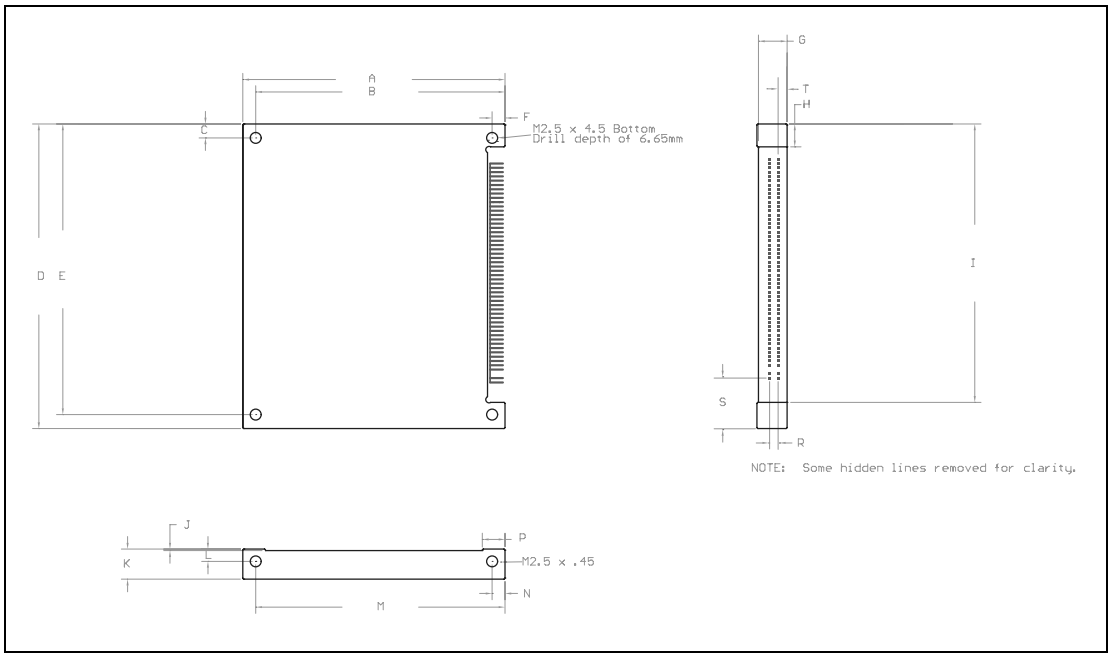

Figure 1: Physical Dimensions

Table 1: Physical Dimensions

Dimension	Millimeters	Tolerance (mm)
A	60.00	±0.25
B	57.05	±0.25
C	3.20	±0.10
D	69.85	±0.25
E	66.65	±0.25
F	2.95	±0.10
G	6.55	±0.125
H	5.25	±0.125
I	63.85	±0.25
J	.35	±0.0125

Dimension	Millimeters	Tolerance (mm)
K	6.90	±0.125
L	2.82	±.10
M	57.05	±0.25
N	2.95	±0.10
P	5.19	±0.125
Q	11.57	±0.125
R	2.00	±0.10
S	11.71	±0.125
T	3.00	±0.10

PIN LOCATIONS

The following diagram identifies the pin locations of the 1.8" Drive.

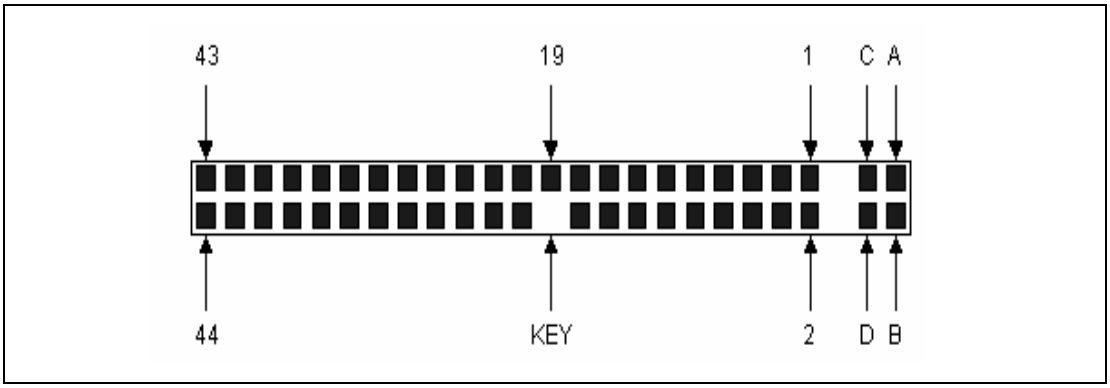

Figure 2: Pin Locations

JUMPER SETTINGS

The following diagram defines the SiliconDrive 1.8" Drive jumper settings.

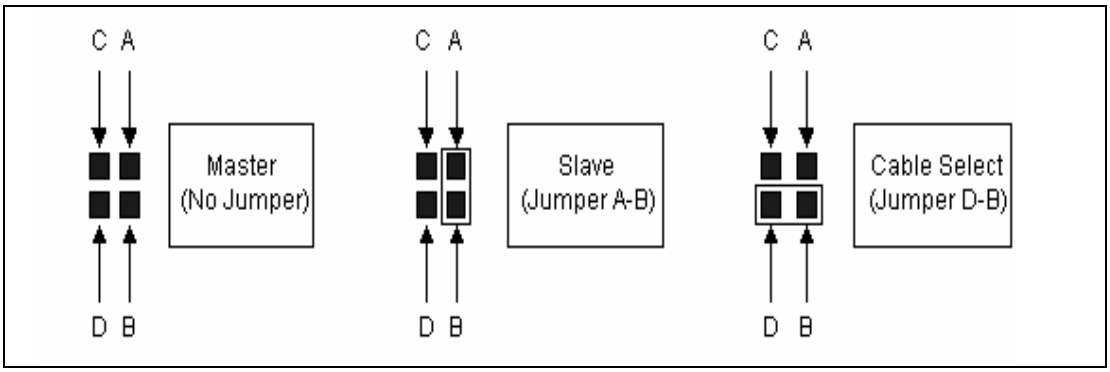

Figure 3: Jumper Settings

PRODUCT SPECIFICATIONS

Note: All SiliconDrive 1.8" Drive values quoted are typical at 25°C and nominal supply voltage.

SYSTEM PERFORMANCE

Table 2: System Performance

Reset to Ready Startup Time (Typical/Maximum)	200ms/400ms
Read Transfer Rate (Typical)	8MBps
Write Transfer Rate (Typical)	6MBps
Burst Transfer Rate	16.7MBps
Controller Overhead (Command to DRQ)	2ms (maximum)

SYSTEM POWER REQUIREMENTS

Note: The 5V is the only operation for the 16GB capacity.

Table 3: System Power Requirements

DC Input Voltage	5.0 ± 10%
Sleep (Standby Current)	>1.0mA
Read (Typical/Peak)	30mA/100mA
Write (Typical/Peak)	40mA/100mA

SYSTEM RELIABILITY

Table 4: System Reliability

MTBF (@ 25ºC)	>4,000,000 hours
Data Reliability	<1 non-recoverable error in 10^{14} bits read
Endurance	>2,000,000 write/erase cycles
Data Retention	10 years

PRODUCT CAPACITY SPECIFICATIONS

Table 5: Product Capacity Specifications

Product Capacity	Formatted Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors/ Track
32MB	32,702,464	63,872	499	2	32
64MB	65,601,536	128,128	1001	4	32
128MB	130,154,496	254,208	993	8	32
256MB	260,571,136	508,928	994	16	32
512MB	521,773,056	1,019,088	1011	16	63
1GB	1,047,674,880	2,046,240	2030	16	63
2GB	2,098,446,336	4,098,528	4066	16	63
4GB	4,224,761,856	8,251,488	8186	16	63
8GB	8,455,200,768	16,514,064	16,383*	16	63
16GB	16,494,428,160	32,215,680	16,383*	16	63

* = All IDE drives 8GB and larger use 16383 cylinders, 16 heads, and 63 sectors/track due to interface restrictions.

ENVIRONMENTAL SPECIFICATIONS

Table 6: Environmental Specifications

Temperature	0ºC to 70ºC (Commercial) -40ºC to 85ºC (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

ELECTRICAL SPECIFICATION

PIN ASSIGNMENTS

The following table describes the SiliconDrive 1.8" Drive 44-pin IDE connector signals.

Table 7: Pin Assignments

Pin	IDE-ATA	Pin	IDE-ATA
1	-RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	KEY
21	DMARQ	22	GND
23	-IOWR	24	GND
25	-IORD	26	GND
27	IORDY	28	-CSEL
29	-DMACK	30	GND
31	INTRQ	32	-IOCS16
33	A1	34	-PDIAG
35	A0	36	A2
37	-CS0	38	-CS1
39	-DASP	40	GND
41	V_{CC}	42	V_{CC}
43	GND	44	NC

SIGNAL DESCRIPTIONS

Table 8: Signal Descriptions

Signal Name	Pin(s)	Type	Description
A2-A0	36, 33, 35	I	**Address Inputs.** These signals are asserted by the host to access the task registers in the device.
-CS0,-CS1	37, 38	I	In the true IDE mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status register and the Device Control register.
-CSEL	28	I	**Cable Select.** This internally pulled-up signal is used to configure this device as a master or a slave when the jumper configuration is in CSEL mode. When this pin is: • Grounded by the host, this device is configured as a master. • Open, this device is configured as a slave.
D15-D0	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	I/O	**Data Inputs/Outputs.** This is the 8-bit or 16-bit bidirectional interface between the host and device. The lower eight bits are used for 8-bit register transfers.
-DMACK	29	I	**DMA Acknowledge.** This signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. When -DMACK is asserted, -CS0 and -CS1 are not asserted and transfers are 16-bits wide.
DASP	39	I/O	**Disk Active/Slave Present.** This open drain output signal is asserted low any time the drive is active. In a master/slave configuration, this signal is used by the slave to inform the master that a slave is present.

Table 8: Signal Descriptions (Continued)

Signal Name	Pin(s)	Type	Description
DMARQ	21	O	**DMA Request.** This signal is used for DMA transfers between the host and device. DMARQ is asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controller by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK (i.e., the device waits until the host asserts -DMACK before negating DMARQ, and reasserts DMARQ if there is more data to transfer). The DMARQ/ -DMACK handshake is used to provide flow control during the transfer.
GND	2, 19, 22, 24, 26, 30, 40, 43	-	**Ground.** The device ground signal.
INTRQ	31	O	**Interrupt Request.** This signal is an active high interrupt request to the host.
IORDY	27	I	**I/O Channel Ready.** The signal is negated to extend the host transfer cycle of any host register access.
-IORD	25	I	**Device I/O Read.** This is the read strobe signal from the host. The falling edge of IORD enables data from the device onto the data bus. The rising edge of IORD latches data at the host. The host does not act on the data until it is latched.
-IOWR	23	I	**Device I/O Write.** This is the write strobe signal from the host. The rising edge of IOWR# latches data from the data bit signals. The device does not act on the data until it is latched.
KEY	20	-	**Key.** Reserved for the Connector Key.
-PDIAG	34	I/O	**Pass Diagnostic.** This open drain signal is asserted by the slave to indicate to the master that it has passed its diagnostics.

Table 8: Signal Descriptions (Continued)

Signal Name	Pin(s)	Type	Description
-RESET	1	I	**Device Reset.** An active low signal. When active, this signal sets all internal registers to their default state. This signal is held asserted until at least 25µs after power has been stabilized during the device power-on.
V_{CC}	41, 42	-	**Device Power Supply.** The device power 5V signal.

ABSOLUTE MAXIMUM RATINGS

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
Ts	Storage Temperature	-55	125	°C
T_A	Operating Temperature	-40	85	°C
V_{CC}	V_{CC} with Respect to GND	-0.3	6.7	V
Vin	Input Voltage	-0.5	6.0	V
Vout	Output Voltage	-0.3	5.8	V

CAPACITANCE

Table 10: Capacitance

Symbol	Parameter	Maximum	Units
Cin	Input Capacitance	35	pF
Cout	Output Capacitance	35	pF
CI/O	Bidirectional Capacitance	35	pF

DC CHARACTERISTICS

Table 11: DC Characteristics

Symbol	Parameter	5V ±10%		Units
		Minimum	Maximum	
V_{CC}	Power Supply Voltage	4.5	5.5	V
I_{LI}	Input Leakage *(1) Current	-	5	µA
I_{LO}	Output Leakage *(1) Current	-	5	µA
V_{CCR}	V_{CC} Read Current	-	80	mA
V_{CCW}	V_{CC} Write Current	-	80	mA
V_{CCS}	V_{CC} Standby Current	-	0.5	mA
V_{IL}	Input Low Voltage	-0.3	0.3 x V_{CC}	V
V_{IH}	Input High Voltage	7 x Vcc	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} - 0.4	-	V

*(1) Except the pulled-up/pulled-down pin.

AC CHARACTERISTICS

I/O Access Read Timing

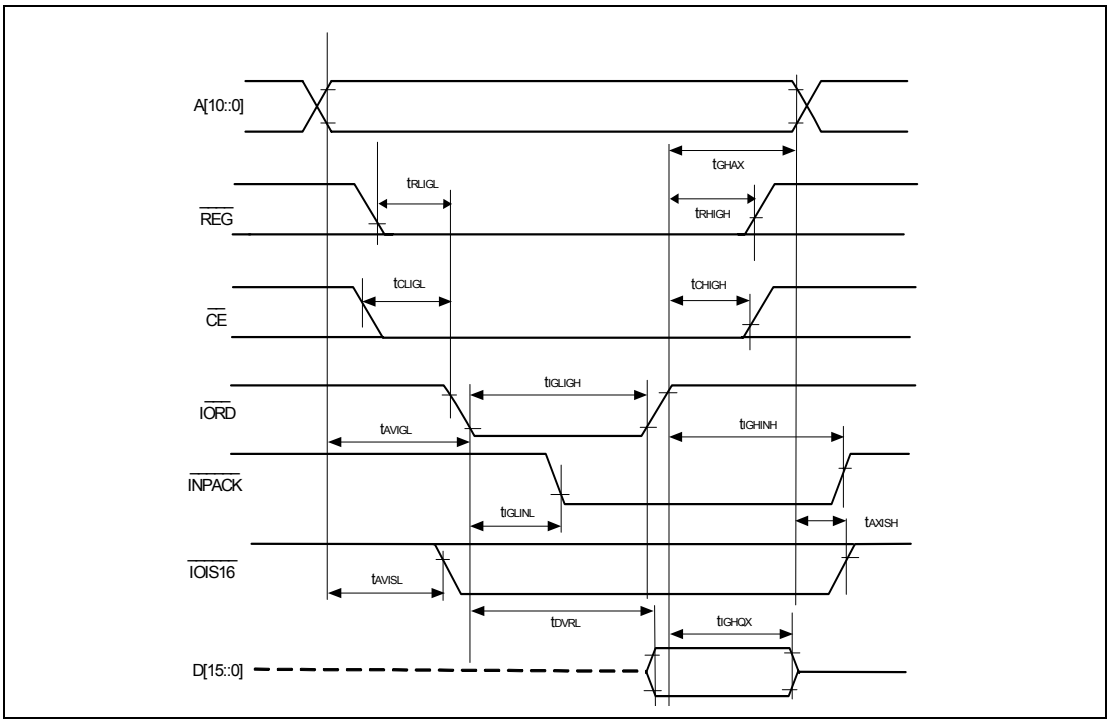

Figure 4: I/O Access Read Timing Diagram

Table 12: I/O Access Read Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{DVRL}	Data Delay after IORD	-	50	ns
t_{IGHQX}	Data Hold following IORD	5	-	ns
t_{IGLIGH}	IORD Pulse Width	65	-	ns
t_{AVIGL}	Address Setup before IORD	25	-	ns
t_{GHAX}	Address Hold following IORD	10	-	ns
t_{CLIGL}	CE Setup before IORD	5	-	ns
t_{CHIGH}	CE Hold following IORD	10	-	ns
t_{RLIGL}	REG Setup before IORD	5	-	ns
t_{RHIGH}	REG Hold following IORD	0	-	ns
t_{IGLINL}	INPACK Delay falling from IORD	-	(1)	ns
t_{IGHINH}	INPACK Delay Rising from IORD	-	(1)	ns
t_{AVISL}	IOIS16 Delay Falling from Address	-	(1)	ns
t_{AXISH}	IOIS16 Delay Rising from Address	-	(1)	ns

Note: (1) IOIS16 and INPACK are not supported.

I/O Access Write Timing

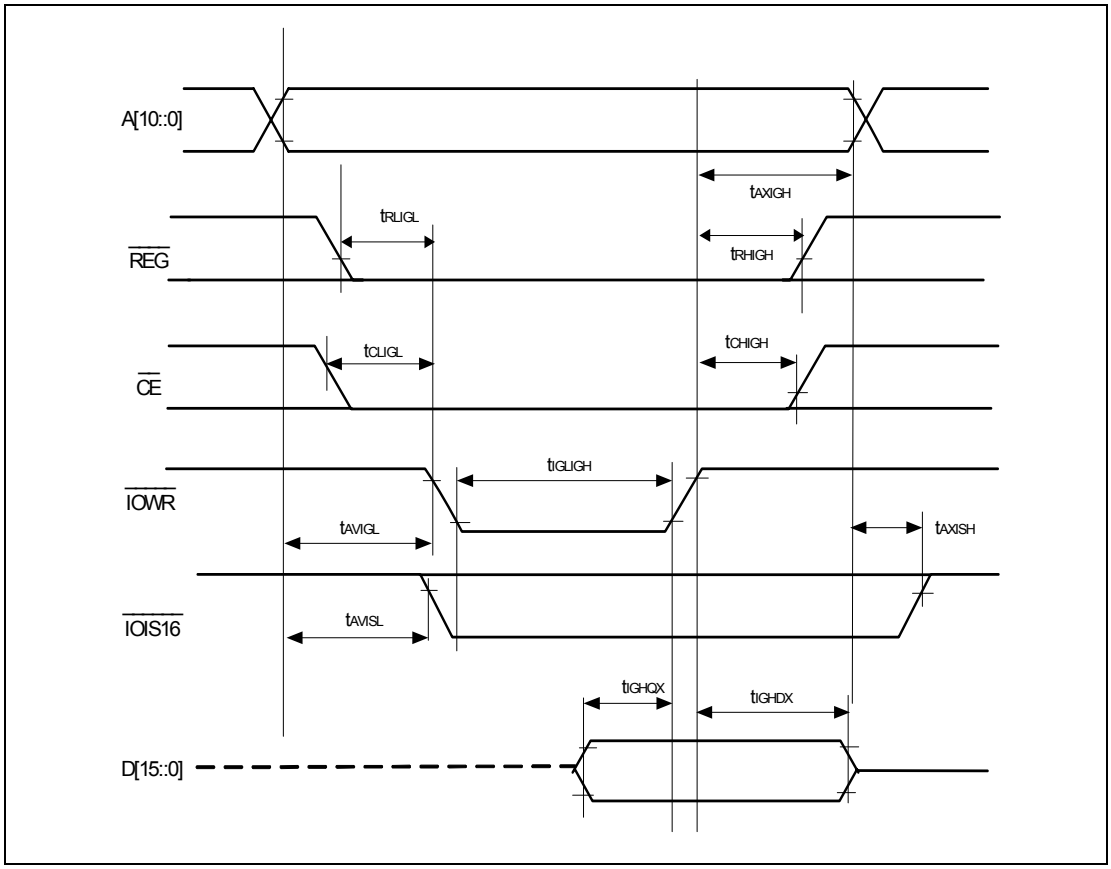

Figure 5: I/O Access Write Timing Diagram

Table 13: I/O Access Write Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{IGHDX}	Data Hold following IOWR	5	-	ns
t_{IGHQX}	Data Setup before IOWR	20	-	ns
t_{IGLIGH}	IOWR Pulse Width	65	-	ns
t_{AVIGL}	Address Setup before IOWR	25	-	ns
t_{AXIGH}	Address Hold following IOWR	10	-	ns
t_{CLIGL}	CE Setup before IOWR	5	-	ns
t_{CHIGH}	CE Hold following IOWR	10	-	ns
t_{RLIGL}	REG Setup before IOWR	5	-	ns
t_{RHIGH}	REG Hold following IOWR	0	-	ns
t_{AVISL}	IOIS16 Delay Falling from Address	-	(1)	ns
t_{AXISH}	IOIS16 Delay Rising from Address	-	(1)	ns

Note: (1) IOIS16 and INPACK are not supported.

True IDE Read/Write Access Timing

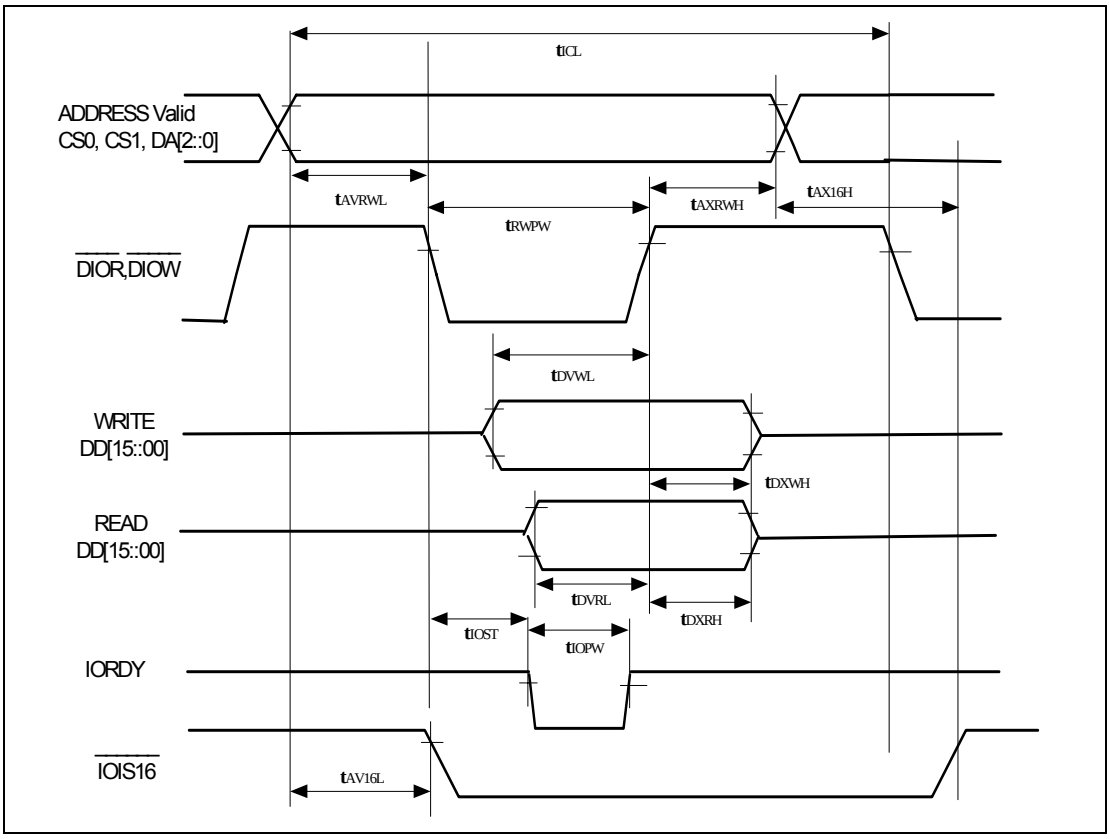

Figure 6: True IDE Read/Write Access Timing Diagram

Table 14: True IDE Read/Write Access Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{ICL}	Cycle Time	100	-	ns
t_{AVRWL}	Address Valid to DIOR,DIOW Setup Time	15	-	ns
t_{RWPW}	DIOR, DIOW Pulse Width	65	-	ns
t_{DVWL}	DIOW Data Setup Time	20	-	ns
t_{DXWH}	DIOW Data Hold Time	5	-	ns
t_{DVRL}	DIOR Data Setup Time	15	-	ns
t_{DXRH}	DIOR Data Hold Time	5	-	ns
t_{AV16L}	Address Valid to IOCS16 Assertion	-	(1)	ns
t_{AX16H}	Address Valid to IOCS16 Negation	-	(1)	ns
t_{AXRWH}	DIOW,DIOR to Address Valid Hold Time	10	-	ns
t_{IOST}	IORDY Setup Time	-	(1)	ns
t_{IOPW}	IORDY Pulse Width	-	(1)	ns

Note: (1) IOIS16 and INPACK are not supported.

True IDE Multiword DMA Read/Write Access Timing

This function does not apply to SiliconDrives that have DMA disabled.

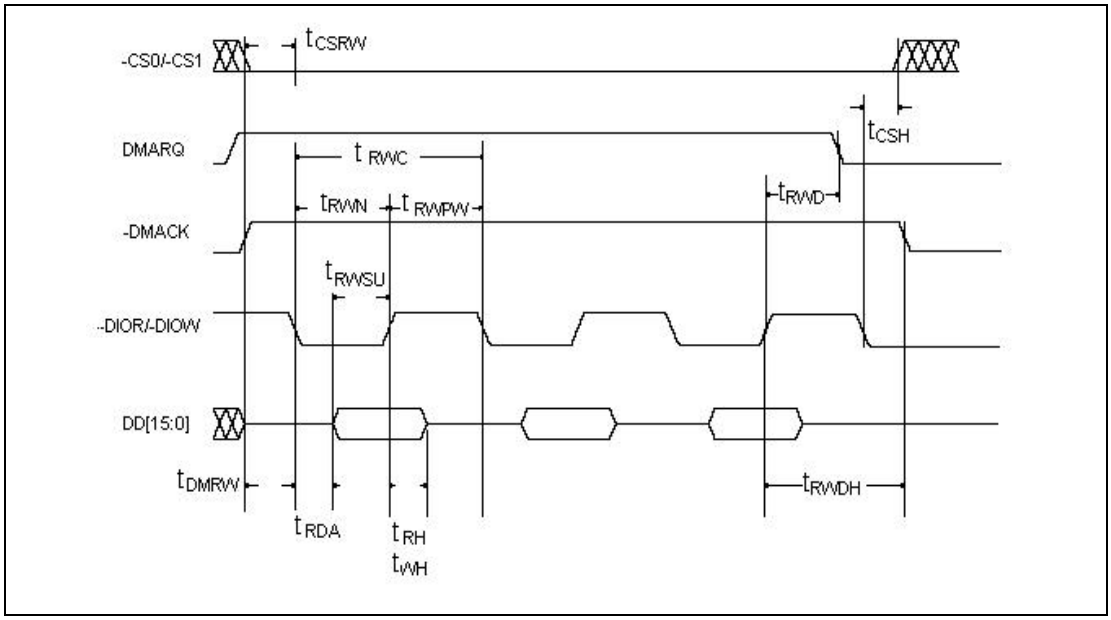

Figure 7: True IDE Multiword DMA Read/Write Access Timing

Table 15: True IDE Multiword DMA Read/Write Access Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{RWC}	Cycle Time (mode 2)	100	-	ns
t_{RWPW}	DIOR/DIOW Pulse Width	65	-	ns
t_{RDA}	DIOR Data Access	-	50	ns
t_{RWSU}	DIOR/DIOW Data Setup Time	15	-	ns
t_{WH}	DIOW Data Hold Time	5	-	ns
t_{RH}	DIOR Data Hold Time	5	-	ns
t_{DMRW}	DMACK to DIOR/DIOW Setup Time	0	-	ns
t_{RWDH}	DIOR/DIOW to DMACK Hold Time	5	-	ns
t_{RWN}	DIOR/DIOW negated Pulse Width	25	-	ns
t_{RWD}	DIOR/DIOW to DMARQ Delay	-	35	ns
t_{CSRW}	CS(1:0) valid to DIOR/DIOW	10	-	ns
t_{CSH}	CS(1:0) Hold Time	10	-	ns

ATA AND TRUE IDE REGISTER DECODING

SiliconDrive can be configured as either a a memory-mapped or an an I/O devices. As noted earlier, communication to and from the drive is accomplished using the ATA Command Block.

TASK FILE REGISTER SPECIFICATION

The Task File registers are used for reading and writing the storage data in the SiliconDrive. The decoded addresses are as shown in the following table.

Table 16: Task File Register Specification

CS0#	CS1#	DA02	DA01	DA00	DIOR# = L	DIOW# = L
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command
0	0	X	X	X	Invalid	Invalid
1	1	X	X	X	High-Z	Not Used
1	0	0	X	X	High-Z	Not Used
1	0	1	0	X	High-Z	Not Used
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used

ATA REGISTERS

DATA REGISTER

The Data register is a 16-bit register used to transfer data blocks between the host and drive buffers. The register may set to 8-bit mode by using the Set Features Command defined in "Seek — 7Xh" on page 45.

ERROR REGISTER

The Error register contains the error status, if any, generated from the last executed ATA command. The contents are qualified by the ERR bit being set in "Status Register" on page 22.

Table 17: Error Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	**Bad Block Detected (BBK).** Set when a bad block is detected.
6	**Uncorrectable Data Error (UNC).** Set when an uncorrectable error is encountered.
5	**Media Changed (MC).** Set to 0.
4	**ID Not Found (IDNF).** Set when the sector ID is not found.
3	**MCR (Media Change Request).** Set to 0.
2	**Aborted Command (ABRT).** Set when a command is aborted due to a drive error.
1	**Track 0 Not Found (TKONF).** Set when the executive drive diagnostic command is executed.
0	**Address Mark Not Found (AMNF).** Set in the case of a general error.

FEATURE REGISTER

The Feature register is command-specific and used to enable and disable interface features. This register supports only either odd or even byte data transfers.

Table 18: Feature Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Feature Byte							

SECTOR COUNT REGISTER

The Sector Count register is used to read or write the sector count of the data for which an ATA transfer has been made.

Table 19: Sector Count Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Count							
Default Value	0	0	0	0	0	0	0	1

SECTOR NUMBER REGISTER

The Sector Number register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence, the device sets the register value to the last sector read or written as a result of the previous AT command.

When Logical Block Addressing (LBA) mode is implemented and the host issues a command, the contents of the register describe the Logical Block Number bits A[7:0]. Following an ATA command, the device loads the register with the LBA block number resulting from the last ATA command.

Table 20: Sector Number Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Number (CHS Addressing)							
	Logical Block Number bits A07-A00 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	1

CYLINDER LOW REGISTER

The Cylinder Low register is set by the host to specify the cylinder number low byte. Following an ATA command, the content of the register is written by the device, identifying the cylinder number low byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Table 21: Cylinder Low Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A15-A08 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

CYLINDER HIGH REGISTER

The Cylinder High register is set by the host to specify the cylinder number high byte. Following an ATA command, the content of the register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Table 22: Cylinder High Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A23-A16 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

DRIVE/HEAD REGISTER

The Drive/Head register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3-0 of the head number in CHS mode or logical block number bits 27-24 in LBA mode.

Table 23: Drive/Head Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	1	LBA	1	DRV	HS3 LBA27	HS2 LBA26	HS1 LBA25	HS0 LBA24
Default Value	1	0	1	0	0	0	0	0

The Drive/Head register is used by the host to specify one of a pair of ATA drives present in the platform.

Bit(s)	Description
6	**LBA.** Selects between CHS (0) and LBA (1) addressing mode.
4	**Drive Address (DRV).** Indicates the drive number selected by the host, either 0 or 1.
3-0	HS3 to 0. Indicates bits 3-0 of the head number in CHS addressing mode or LBA bits 27-24 in LBA mode. • CHS to LBA conversion: LBA = (C x HpC + H) x SpH + S -1 • LBA to CHS conversion: ◦ C = LBA/(HpC x SpH) ◦ H = (LBA/SpH) mod (HpC) ◦ S = (LBA mod(SpH)) + 1 ...where: ◦ C is the cylinder number ◦ H is the head number ◦ S is the sector count ◦ HpC is the head count per cylinder count ◦ SpH is the sector count per head count (track)

STATUS REGISTER

The Status register provides the device's current status to the host. The status register is an 8-bit read-only register. When the contents of the register are read by the host, the IREQ# bit is cleared.

Table 24: Status Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	**Busy (BSY).** Set when the drive is busy and unable to process any new ATA commands.
6	**Data Ready (DRDY).** Set when the device is ready to accept ATA commands from the host.
5	**Drive Write Fault (DWF).** Always set to 0.
4	**Drive Seek Complete (DSC).** Set when the drive heads have been positioned over a specific track.
3	**Data Request (DRQ).** Set when a device is ready to transfer a word or byte of data to or from the host and the device.
2	**Corrected Data (CORR).** Always set to 0.
1	**Index (IDX).** Always set to 0.
0	**Error (ERR).** Set when an error occurs during the previous ATA command.

COMMAND REGISTER

The Command register specifies the ATA command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Table 25: Command Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	ATA Command Code							

See "ATA Command Block and Set Description" on page 27 for a listing of the supported ATA commands.

ALTERNATE STATUS REGISTER

The Alternate Status register is a read-only register indicating the status of the device, following the previous ATA command. See "Status Register" on page 22 for specific details.

Table 26: Alternate Status Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

DEVICE CONTROL REGISTER

The Device Control register is used to control the interrupt request and issue ATA software resets.

Table 27: Device Control Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write	-	-	-	-	1	SRST	nIEN	0

Bit(s)	Description
7-4	Reserved bits.
3	Always set to 1.
2	**Software Reset (SRST).** When set, resets the ATA software.
1	**Interrupt Enable (nIEN).** When set, device interrupts are disabled. There is no function in the memory-mapped mode.
0	Always set to 0.

DEVICE ADDRESS REGISTER

The Device Address register is used to maintain compatibility with ATA disk drive interfaces.

Table 28: Device Address Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	-	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Default Value	0	0	1	1	1	1	1	0

Bit(s)	Description
7	Reserved bit.
6	**Write Gate (nWTG).** Low when a write to the device is in process.
5-2	**nHS3 to nHS0.** The negated binary address of the currently selected head.
1	**nDS1.** Low when drive 1 is selected and active.
0	**nDS0.** Low when drive 0 is selected and active.

ATA COMMAND BLOCK AND SET DESCRIPTION

In accordance with the *ANSI ATA Specification*, the device implements seven registers that are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol. A description of the ATA command block is provided in the following table.

Table 29: ATA Command Block and Set Description

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	X							

ATA COMMAND SET

Table 30: ATA Command Set

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98h, E5h	-	-	-	-	D	-
1	Execute Drive Diagnostics	90h	-	-	-	-	D	-
1	Erase Sector	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	97h, E3h	-	Y	-	-	D	-
1	Idle Immediate	95h, E1h	-		-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA*	C8h	-	Y	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y

Table 30: ATA Command Set (Continued)

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Read Long Sector	22h, 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h, 21h	-	-	Y	Y	Y	Y
1	Read Verify Sector(s)	40h, 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	Y	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y		-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	99h, E6h	-	-	-	-	D	-
1	Standby	96h, E2h	-	-	-	-	D	-
1	Standby Immediate	94h, E0h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
1	Write DMA*	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h, 33h	-		Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h, 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

* = This function does not apply to SiliconDrives that have DMA disabled.

Notes:

- CY = Cylinder
- SC = Sector Count
- DH = Drive/Head
- SN = Sector Number
- FR = Feature LBA — LBA bit of the Drive/Head register (D denotes that only the drive bit is used)

Check Power Mode — 98h, E5h

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode or is entering or exiting standby, the BSY bit is set, the Sector Count register set to 00h, and the BSY bit is cleared. In idle mode, BSY is set and the Sector Count register is set to FFh. The BSY bit is then cleared and an interrupt is issued.

Table 31: Check Power Mode — 98h, E5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	98h or E5h							

Executive Drive Diagnostic — 90h

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55AAh). If an error is detected in the read/write buffer, the Error register reports the appropriate diagnostic code.

Table 32: Executive Drive Diagnostic — 90h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	90h							

Format Track — 50h

The Format Track command formats the common solid-state memory array.

Table 33: Format Track — 50h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	50h							

Identify Drive — ECh

Issued by the host, the Identify Drive command provides 256 bytes of drive attribute data (i.e., sector size, count, and so on) The identify drive data structure is detailed in the following table.

Table 34: Identify Drive — ECh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	ECh							

Identify Drive — Drive Attribute Data

Table 35: Identify Drive — Drive Attribute Data

Word Address	Data Default	Bytes	Data Description
0	045Ah	2	General configuration bit information • 15: Non-magnetic disk • 14: Formatting speed latency permissible gap needed • 13: Track Offset option supported • 12: Data Strobe Offset option supported • 11: Over 0.5% rotational speed difference • 10: Disk transfer rate >10Mbps • 9: 10Mbps >= disk transfer rate >5Mbps • 8: 5Mbps >= disk transfer rate • 7: Removable cartridge drive • 6: Fixed drive • 5: Spindle Motor Control option executed • 4: Over 15µs changing head time • 3: Non-MFM encoding • 2: Soft sector allocation • 1: Hard sector allocation • 0: Reserved
1	XXXXh	2	Number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of heads
4	0000h	2	Number of unformatted bytes per track
5	XXXXh	2	Number of unformatted bytes per sector
6	XXXXh	2	Number of sectors per track
7-8	XXXXh	4	Number of sectors per device
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number

Table 35: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
20	0001h	2	Buffer type • 0000h: Not specified • 0001h: A single-ported, single-sector buffer • 0002h: A dual-ported multisector buffer • 0003h: A dual-ported multisector buffer with a read caching
21	0001h	2	Buffer size in 512-byte increments
22	0004h	2	Number of ECC bytes passed on read/ write long commands
23-26	XXXXh	8	Firmware revision (eight ASCII characters)
27-46	XXXXh	40	Model number (40 ASCII characters)
47	0001h	2	7-0: Maximum number of sectors that can be transferred with a Read/Write Multiple command per interrupt
48	0000h	2	Double word (32 bit) not supported
49	0f00h	2	• 11: IORDY supported • 9: LBA supported • 8: DMA supported
50	0000h	2	Reserved
51	0200h	2	15-8: PIO data transfer cycle timing
52	0000h	2	15-8: DMA data transfer cycle timing
53	0003h	2	• 1: Words 64-70 are valid • 0: Words 54-58 are valid
54	XXXXh	2	Current number of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors
59	010Xh	2	7-0: Current sectors can be transferred with a Read/Write Multiple command per interrupt
60-61	XXXXh	4	Total number of sectors addressable in LBA mode
62	0000h	2	Single-word DMA modes supported

Idle — 97h, E3h

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5ms, and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

Table 36: Idle — 97h, E3h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count (5ms increments)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	97h or E3h							

Idle Immediate — 95h, E1h

When issued by the host, the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

Table 37: Idle Immediate — 95h, E1h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	95h or E1h							

Initialize Drive Parameters — 91h

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to 1 Fixed. Upon issuance of the command, the device sets the BSY bit and associated parameters, clears the BSY bit, and issues an interrupt.

Table 38: Initialize Drive Parameters — 91h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count (Number of Sectors)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	0	X	Drive	Head Number (Number of Heads — 1)			
Command	91h							

Recalibrate — 1Xh

The Recalibrate command sets the cylinder low and high, head number to 0h, and sector number to 1h in CHS mode. In LBA mode (i.e., LBA = 1), the sector number is set to 0h.

Table 39: Recalibrate — 1Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	1Xh							

Read Buffer — E4h

The Read Buffer command allows the host to read the contents of the sector buffer. When issued, the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. When the data is ready, the DRQ bit is set and the BSY bit in the Status register are set and cleared, respectively.

Table 40: Read Buffer — E4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E4h							

Read DMA — C8h

The Read DMA command allows the host to read data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrives that have DMA disabled.

Table 41: Read DMA — C8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C8h							

Read Multiple — C4h

The Read Multiple command executes similarly to the Read Sector command, with the exception that interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

Table 42: Read Multiple — C4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C4h							

Read Sector — 20h, 21h

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count register. If the sector count is set to 0h, all 256 sectors of data are made available. When the command code is issued and the first sector of data has been transferred to the buffer, the DRQ bit is set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

Table 43: Read Sector — 20h, 21h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	20h or 21h							

Read Long Sector(s) — 22h, 23h

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

Table 44: Read Long Sector(s) — 22h, 23h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	22h or 23h							

Read Verify Sector(s) — 40h, 41h

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that is does not set the DRQ bit and does not transfer data to the host. When the requested sectors are verified, the onboard controller clears the BSY bit and issues an interrupt.

Table 45: Read Verify Sector(s) — 40h, 41h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	40h or 41h							

Seek — 7Xh

The Seek command seeks and picks up the head to the tracks specified in the task file. When the command is issued, the solid-state memory chips do not need to be formatted. After an appropriate amount of time, the DSC bit is set.

Table 46: Seek — 7Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	7Xh							

Set Features — EFh

The Set Features command allows the host to configure the feature set of the device according to the attributes listed in Table 48.

Table 47: Set Features — EFh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	Feature							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	EFh							

Table 48: Set Features' Attributes

Feature	Operation
01h	Enable 8-bit data transfer
66h	Disable reverting to power on defaults
81h	Disable 8-bit data transfer
BBh	4 bytes of data apply on Read/Write Long commands
CCh	Enable revert to power on defaults

On power-up or following a hardware reset, the device is set to the default mode 81h.

Set Multiple Mode — C6h

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

Table 49: Set Multiple Mode — C6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	C6h							

Set Sleep Mode — 99h, E6h

The Set Sleep Mode command allows the host to set the device in sleep mode. When the onboard controller transitions to sleep mode, it clears the BSY bit and issues an interrupt. The device interface then becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

Table 50: Set Sleep Mode — 99h, E6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	99h or E6h							

Standby — 96h, E2h

When the Standby command is issued by the host, it transitions the device into standby mode. If the Sector Count register is set to a value other than 0h, the Auto Powerdown function is enabled and the device returns to Idle mode.

Table 51: Standby — 96h, E2h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count (5ms x Timer Count)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	96h or E2h							

Standby Immediate — 94h, E0h

When the Standby Immediate command is issued by the host, it transitions the device into standby mode.

Table 52: Standby Immediate — 94h, E0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_7
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	94h or E0h							

Write Buffer — E8h

The Write Buffer command allows the host to rewrite the contents of the 512- byte data buffer with the wanted data.

Table 53: Write Buffer — E8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_7
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E8h							

Write DMA — CAh

The Write DMA command allows the host to write data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrives that have DMA disabled.

Table 54: Write DMA — CAh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	CAh							

Write Multiple — C5h

The Write Multiple command operates in the same manner as the Write Sector command. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 55: Write Multiple — C5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	C5h							

Write Sector(s) — 30h, 31h

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 56: Write Sector(s) — 30h, 31h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	30h or 31h							

Write Long Sector(s) — 32h, 33h

The Write Long Sector(s) command operates in the same manner as the Write Sector command — when issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 57: Write Long Sector(s) — 32h, 33h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	32h or 33h							

Erase Sector(s) — C0h

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

Table 58: Erase Sector(s) — C0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	C0h							

Request Sense — 03h

The Request Sense command identifies the extended error codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error register.

Table 59: Request Sense — 03h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	X	1	Drive	X			
Command	03h							

The extended error codes are defined in the following table.

Table 60: Extended Error Codes

Extended Error Codes	Description
00h	No error detected
01h	Self test is OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (requested head or sector invalid)
2Fh	Address overflow (address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30h-32h, 37h,3Eh	Self test of diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Computed media format
03h	Write/erase failed

Translate Sector — 87h

The Translate Sector command is not currently supported by the SiliconSystems' SiliconDrive. If the host issues this command, the device responds with 0x00h in the data register.

Table 61: Translate Sector — 87h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	87h							

Wear-Level — F5h

The Wear-Level command is supported as an NOP command for the purposes of backward compatibility with the ANSI AT attachment standard. This command sets the Sector Count register to 0x00h.

Table 62: Wear-Level — F5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Completion Status							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	Flag			
Command	F5h							

Write Multiple w/o Erase — CDh

The Write Multiple w/o Erase command functions identically to the Write Multiple command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 63: Write Multiple w/o Erase — CDh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	CDh							

Write Sector(s) w/o Erase — 38h

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 64: Write Sector(s) w/o Erase — 38h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	38h							

Write Verify — 3Ch

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command, with the added feature of verifying each sector written.

Table 65: Write Verify — 3Ch

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	3Ch							

SALES AND SUPPORT

To order or obtain information on pricing and delivery, contact your SiliconSystems Sales Representative.

PART NUMBERING

NOMENCLATURE

The following table defines the SiliconDrive 1.8" Drive part numbering scheme.

Table 66: Part Numbering Nomenclature

SSD-	**H**	**YYY**	**T**	**-3650** Part number suffix — contact your SiliconSystems' Sales Representative
			Temperature Range: • Blank = Commercial • I = Industrial	
		Capacity: 32M = 32MB to 16G = 16GB		
	Form Factor: • C = CF • D = 2.5" Drive • H = 1.8" Drive • M = Module • P = PC Card			
SiliconSystems' **S**ilicon**D**rive				

PART NUMBERS

The following table lists the SiliconDrive's part numbers.

Table 67: Part Numbers

Part Number	Capacity
SSD-H16G(I)-3650	16GB
SSD-H08G(I)-3650	8GB
SSD-H04G(I)-3650	4GB
SSD-H02G(I)-3650	2GB
SSD-H01G(I)-3650	1GB
SSD-H51M(I)-3650	512MB
SSD-H25M(I)-3650	256MB
SSD-H12M(I)-3650	128MB
SSD-H64M(I)-3650	64MB
SSD-H32M(I)-3650	32MB

ROHS 6 OF 6 PRODUCT LABELING — PB-FREE IDENTIFICATION LABEL

The Pb-free identification label indicates that the enclosed components/ devices and/or assemblies do not contain any lead (i.e., they are lead-free, as defined in RoHS directive 2002/95/ED). The above symbol is on all RoHS 6 of 6 compliant product labels, as seen in Figure 8.

SAMPLE LABEL

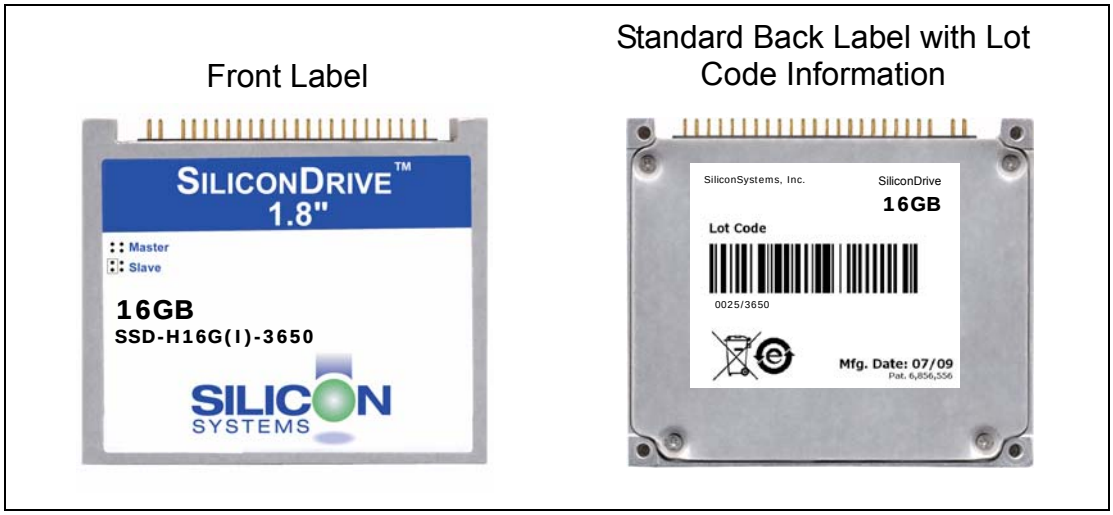

Figure 8: Sample Label

RELATED DOCUMENTATION

For more information, visit www.siliconsystems.com or contact your SiliconSystems Sales Representative.

Table 68: Related Documentation

SiliconDrive Application-Specific Technology	Description	Document Number
PowerArmor	Eliminates drive corruption	SSWPxx-PowerArmor-R
SiProtect	Protection software for password-required, read/write, or read-only access.	SSANxx-SilDrvSec-R
SiSweep	Ultra-fast data erasure	SSANxx-SilDrvSec-R
SiPurge	Non-recoverable data erasure	SSANxx-SilDrvSec-R

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