DATA SHEET

SILICONDRIVE II 2.5" PATA DRIVE

SSD-DXXX(I)-4300

OVERVIEW

The SiliconDrive II 2.5" PATA Drive is an optimal time-to-market replacement for hard drives and flash cards or in host systems that require low power and scalable storage solutions.

SiliconDrive II technology is engineered exclusively for the high performance, high reliability and multi-year product lifecycle requirements of the Enterprise System OEM market. Typical end-market applications include broadband data and voice networks, military systems, flight system avionics, medical equipment, industrial control systems, video surveillance, storage networking, VoIP, wireless infrastructure, and interactive kiosks.

Every SiliconDrive II 2.5" PATA Drive is integrated with SiliconSystems patented PowerArmor and patent-pending SiSMART and SiSecure technologies.

PowerArmor prevents data corruption and loss from power disturbances by integrating patented technology into every SiliconDrive II.

SiSMART acts as an early warning system to eliminate unscheduled downtime by constantly monitoring and reporting the exact amount of remaining storage system useful life.

SiSecure is a comprehensive suite of user-selectable security technologies that solves the critical need for robust storage security for embedded systems applications that have a small footprint and low-power requirement.

SISECURE

SiZone	Data zones with different security parameters.
SiKey	Ties SiliconDrive to a specific host and/or software IP.
SiProtect	Protection software for password-required, read/write, or read-only access.
SiSweep	Ultra-fast data erasure.
SiPurge	Non-recoverable data erasure.
AutoLock	Automatically locks the SiliconDrive.

FEATURES

- RoHS 6 of 6 compliant
- Integrated PowerArmor, SiSMART, and SiSecure technology
- Capacity range: 4GB to 32GB
- MTBF 4,000,000 hours

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REVISION HISTORY

Document No.	Release Date	Changes
4300D-00DSR	February 27, 2009	Initial release.

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PHYSICAL SPECIFICATIONS

The SiliconDrive II 2.5" PATA Drive products are offered in an industry-standard 2.5" PATA Drive form factor. See "Part Numbering" on page 77 for details regarding 2.5" PATA Drive capacities.

PHYSICAL DIMENSIONS

This section provides diagrams that describe the physical dimensions for the 2.5" PATA Drive.

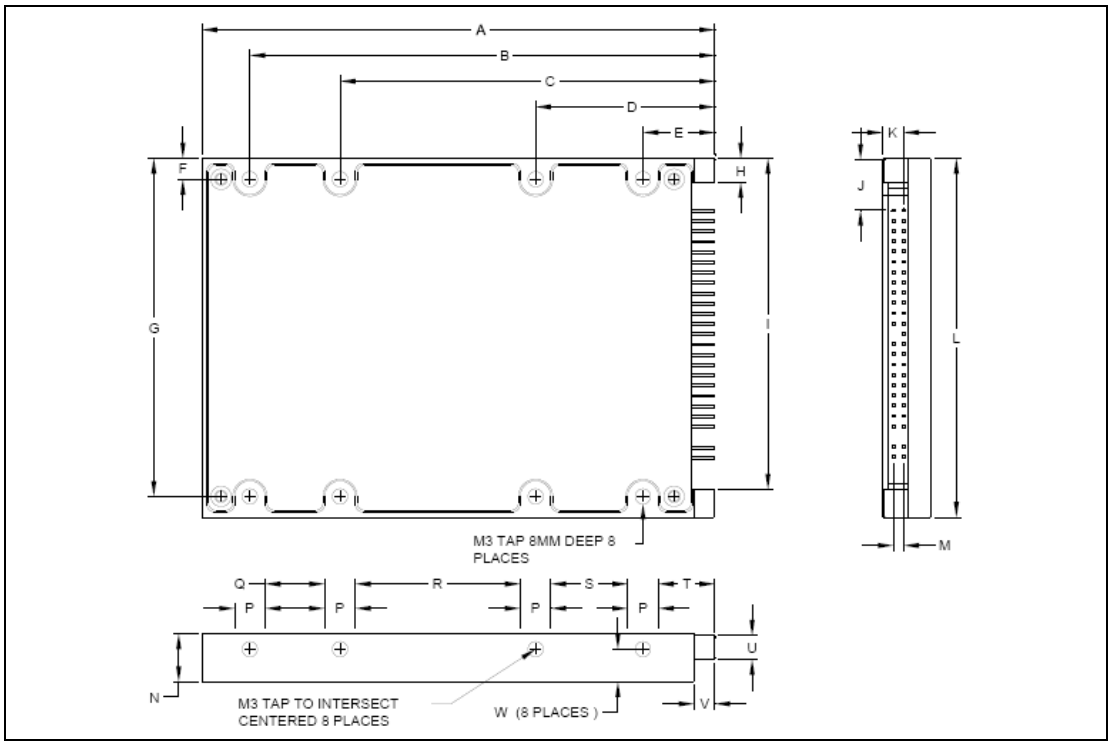

Figure 1: Physical Dimensions

Dimension	Millimeters	Tolerance (mm)
A	100.00	±0.25
B	90.60	±0.125
C	73.03	±0.125
D	34.93	±0.125
E	14.00	±0.125
F	4.08	±0.125
G	61.70	±0.125
H	4.68	±0.125
I	64.42	±0.125
J	10.14	±0.51
K	3.99	±0.43

Dimension	Millimeters	Tolerance (mm)
L	69.85	±0.25
M	2.00	±0.125
N	9.40	±0.10
P	6.00	±0.125
Q	11.57	±0.125
R	32.10	±0.125
S	14.93	±0.125
T	11.00	±0.125
U	4.65	±0.125
V	4.00	±0.125
W	6.15	±0.125

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PIN LOCATIONS

The following diagram identifies the pin locations of the 2.5" PATA Drive.

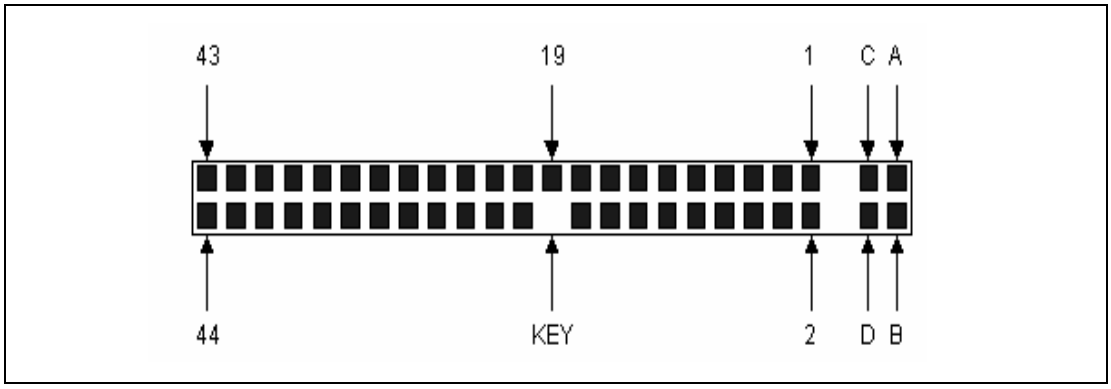

Figure 2: Pin Locations

JUMPER SETTINGS

The following diagram defines the SiliconDrive II 2.5" PATA Drive jumper settings.

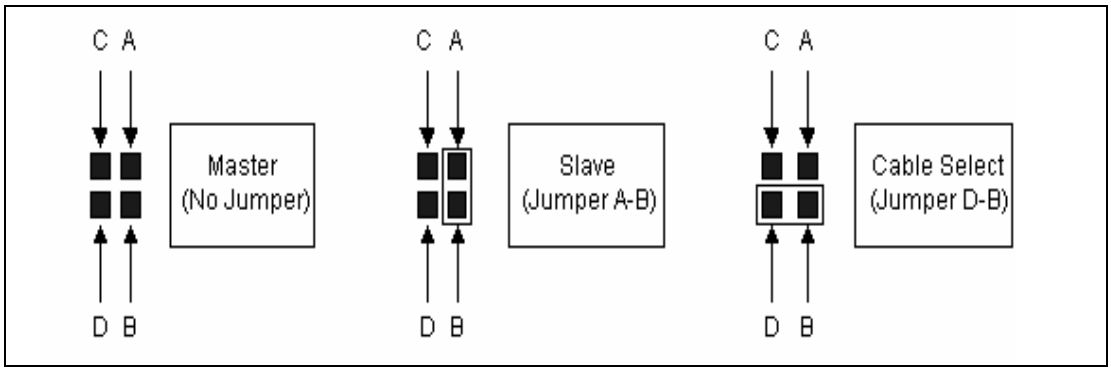

Figure 3: Jumper Settings

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PRODUCT SPECIFICATIONS

Note: All SiliconDrive II 2.5" PATA Drive values quoted are typical at 25°C and nominal supply voltage.

SYSTEM PERFORMANCE

Table 1: System Performance

Reset to Ready Startup Time (Typical/Maximum)	200ms/400ms
Read Transfer Rate (Typical)	34MBps
Write Transfer Rate (Typical)	19MBps
Burst Transfer Rate	66MBps
Controller Overhead (Command to DRQ)	2ms (maximum)

SYSTEM POWER REQUIREMENTS

Table 2: System Power Requirements

DC Input Voltage	5.0 ± 10%
Sleep (Standby Current)	1.0mA
Read (Typical/Peak)	60mA/120mA
Write (Typical/Peak)	60mA/120mA

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RELIABILITY

Table 3: Reliability

MTBF (@ 25ºC)	4,000,000 hours
Bit Error Rate	<1 non-recoverable error in 10^{14} bits read

PROJECTED OPERATIONAL LIFE SPAN

Table 4: Operational Life Span

SiliconDrive Part#	Capacity	Service Life*		GB Written per Day
SSD-D032G-4300	32GB	217.6 Years	@	402.9GB
SSD-D016G-4300	16GB	108.8 Years	@	402.9GB
SSD-D008G-4300	8GB	54.4 Years	@	402.9GB
SSD-D004G-4300	4GB	27.2 Years	@	402.9GB

* There are unlimited read cycles. Service life is determined using SiliconSystems' LifeEST calculation at 100% duty cycle with 25% write cycles.

LifeEST is a comprehensive measurement that considers numerous factors to determine the projected life span of a SiliconDrive. A white paper that describes the benefits of LifeEST and how to calculate it can be found at http://www.siliconsystems.com/resources/Documents/Whitepaper/SiliconSystems_NAND_Evolution.pdf.

The actual life of a SiliconDrive is dependant on the customer usage model. SiSMART is a patented technology of SiliconSystems that enables host systems to monitor actual usage of a SiliconDrive in real time. SiSMART measures and reports the remaining life of a SiliconDrive. For more information on SiSMART, refer to the *Eliminating Unscheduled Downtime by Forecasting Useable Life* white paper at http://www.siliconsystems.com/technology/pdfs/SiliconDrive_SiSMART.pdf.

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PRODUCT CAPACITY SPECIFICATIONS

Table 5: Product Capacity Specifications

Product Capacity	Capacity (Bytes)	Number of Sectors	Number of Cylinders	Number of Heads	Number of Sectors/ Track
4GB	4,110,188,544	8,027,712	7964	16	63
8GB	8,195,604,480	16,007,040	15,880	16	63
16GB	16,391,208,960	32,014,080	16,383	16	63
32GB	32,782,417,920	64,028,160	16,383	16	63

ENVIRONMENTAL SPECIFICATIONS

Table 6: Environmental Specifications

Temperature	0ºC to 70ºC (Commercial) -40ºC to 85ºC (Industrial)
Humidity	8% to 95% non-condensing
Vibration	16.3gRMS, MIL-STD-810F, Method 514.5, Procedure I, Category 24
Shock	1000G, Half-sine, 0.5ms Duration 50g Pk, MIL-STD-810F, Method 516.5, Procedure I
Altitude	80,000ft, MIL-STD-810F, Method 500.4, Procedure II

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ELECTRICAL SPECIFICATION

PIN ASSIGNMENTS

The following table describes the SiliconDrive II 2.5" PATA Drive 44-pin IDE connector signals.

Table 7: Pin Assignments

Pin	IDE-ATA	Ultra DMA	Pin	IDE-ATA	Ultra DMA
1	RESET#	RESET#	2	GND	GND
3	D7	D7	4	D8	D8
5	D6	D6	6	D9	D9
7	D5	D5	8	D10	D10
9	D4	D4	10	D11	D11
11	D3	D3	12	D12	D12
13	D2	D2	14	D13	D13
15	D1	D1	16	D14	D14
17	D0	D0	18	D15	D15
19	GND	GND	20	KEY	KEY
21	DMARQ	DMARQ#	22	GND	GND
23	IOWR#	STOP	24	GND	GND
25	IORD#	HDSTROBE HDMARDY#	26	GND	GND
27	IORDY	DDSTROBE DDMARDY#	28	CSEL#	CSEL#
29	DMACK#	DMACK#	30	GND	GND
31	INTRQ	INTRQ	32	IOCS16#	IOCS16#
33	A1	A1	34	PDIAG#	PDIAG#
35	A0	A0	36	A2	A2
37	CS0#	CS0#	38	CS1#	CS1#
39	DASP#	DASP	40	GND	GND
41	V_{CC}	V_{CC}	42	V_{CC}	V_{CC}
43	GND	GND	44	NC	NC

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SIGNAL DESCRIPTIONS

Table 8: Signal Descriptions

Signal Name	Pin(s)	Type	Description
A2-A0	36, 33, 35	I	**Address Inputs.** These signals are asserted by the host to access the task registers in the device.
-CS0,-CS1	37, 38	I	In the true IDE mode, -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status register and the Device Control register.
-CSEL	28	I	**Cable Select.** This internally pulled-up signal is used to configure this device as a master or a slave when the jumper configuration is in CSEL mode. When this pin is: • Grounded by the host, this device is configured as a master. • Open, this device is configured as a slave.
D15-D0	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	I/O	**Data Inputs/Outputs.** This is the 8-bit or 16-bit bidirectional interface between the host and device. The lower eight bits are used for 8-bit register transfers.
-DMACK	29	I	**DMA Acknowledge.** This signal is used by the host in response to DMARQ to initiate DMA transfers. The DMARQ/-DMACK handshake is used to provide flow control during the transfer. When -DMACK is asserted, -CS0 and -CS1 are not asserted and transfers are 16-bits wide.
DASP	39	I/O	**Disk Active/Slave Present.** This open drain output signal is asserted low any time the drive is active. In a master/slave configuration, this signal is used by the slave to inform the master that a slave is present.

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Table 8: Signal Descriptions (Continued)

Signal Name	Pin(s)	Type	Description
DMARQ	21	O	**DMA Request.** This signal is used for DMA transfers between the host and device. DMARQ is asserted by the device when the device is ready to transfer data to/from the host. The direction of data transfer is controller by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK (i.e., the device waits until the host asserts -DMACK before negating DMARQ, and reasserts DMARQ if there is more data to transfer). The DMARQ/-DMACK handshake is used to provide flow control during the transfer.

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Table 8: Signal Descriptions (Continued)

Signal Name	Pin(s)	Type	Description
DMARQ# (UDMA protocol active)			This signal is a DMA request that is used for DMA data transfers between the host and device. This signal is asserted by the device when it is ready to transfer data to or from the host. For Multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. This signal is used in a handshake manner with -DMACK (i.e., the device waits until the host asserts (-)DMACK before negating (-)DMARQ, and reasserts (-)DMARQ if there is more data to transfer). In PCMCIA I/O mode, the -DMARQ is ignored by the host while the host is performing an I/O Read cycle to the device. The host does not initiate an I/O Read cycle while -DMARQ is asserted by the device. In True IDE mode, DMARQ is not driven when the device is not selected in the Drive-Head register. While a DMA operation is in progress, -CS0 (-CE1) and -CS1 (-CE2) are held negated and the width of the transfers is 16 bits. If there is no hardware support for True IDE DMA mode in the host, this output signal is not used and should not be connected at the host. In this case, the BIOS must report that DMA mode is not supported by the host so that device drivers do not attempt the DMA mode operation.
GND	2, 19, 22, 24, 26, 30, 40, 43	-	**Ground.** The device ground signal.
INTRQ	31	O	**Interrupt Request.** This signal is an active high interrupt request to the host.

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Table 8: Signal Descriptions (Continued)

Signal Name	Pin(s)	Type	Description
IORDY (True IDE mode)	27	I	**I/O Channel Ready.** The signal is negated to extend the host transfer cycle of any host register access.
-IORD (True IDE mode)	25	I	**Device I/O Read.** This is the read strobe signal from the host. The falling edge of IORD enables data from the device onto the data bus. The rising edge of IORD latches data at the host. The host does not act on the data until it is latched.
-DDMARDY (UDMA write protocol active)			When UDMA mode DMA write is active in all modes, this signal is asserted by the device during a data burst to indicate that the device is ready to receive UDMA data-out bursts. The device may negate -DDMARDY to pause a UDMA transfer.
DSTROBE (UDMA read protocol active)			When UDMA mode DMA read is active in all modes, this signal is the data in strobe generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause a UDMA data-in burst.
-IOWR (True IDE mode)	23	I	**Device I/O Write.** This is the write strobe signal from the host. The rising edge of IOWR# latches data from the data bit signals. The device does not act on the data until it is latched.
-HDMARDY (UDMA read protocol active)			When UDMA mode DMA read is active in all modes, this signal is asserted by the host to indicate that the host is ready to receive UDMA data-in bursts. The host may negate -HDMARDY to pause a UDMA transfer.

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Table 8: Signal Descriptions (Continued)

Signal Name	Pin(s)	Type	Description
HDSTROBE (UDMA write protocol active)			When UDMA mode DMA write is active in all modes, this signal is the data-out strobe generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an UDMA data-out burst.
KEY	20	-	**Key.** Reserved for the Connector Key.
STOP (UDMA protocol active)			While the UDMA mode protocol is active in all modes, the assertion of this signal causes the termination of the UDMA data burst.
-PDIAG	34	I/O	**Pass Diagnostic.** This open drain signal is asserted by the slave to indicate to the master that it has passed its diagnostics.
-RESET	1	I	**Device Reset.** An active low signal. When active, this signal sets all internal registers to their default state. This signal is held asserted until at least 25µs after power has been stabilized during the device power-on.
V_{CC}	41, 42	-	**Device Power Supply.** The device power +3.3V/5V signal.

ABSOLUTE MAXIMUM RATINGS

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
T_S	Storage Temperature	-55	125	°C
T_A	Operating Temperature	-40	85	°C
V_{CC}	V_{CC} with Respect to GND	-0.5	V_{CC} + 0.5	V
V_{IN}	Input Voltage	-0.3	V_{CC} + 0.3	V
V_{OUT}	Output Voltage	-	6.0	V

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DC CHARACTERISTICS

Table 10: DC Characteristics

Symbol	Parameter	5V ± 10%		Units
		Minimum	Maximum	
I_{LI}	Input Leakage *(1) Current	-	10	µA
I_{LO}	Output Leakage *(1) Current	-	10	µA
I_{CCR}	I_{CC} Read Current	60	120	mA
I_{CCW}	I_{CC} Write Current	60	120	mA
I_{CCS}	I_{CC} Standby Current	-	<1.0	mA
V_{IL}	Input Low Voltage	-0.3	V_{CC} x 0.3	V
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	-	0.45	V
V_{OH}	Output High Voltage	2.4	-	V

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AC CHARACTERISTICS

True IDE PIO Mode Read/Write Access Timing

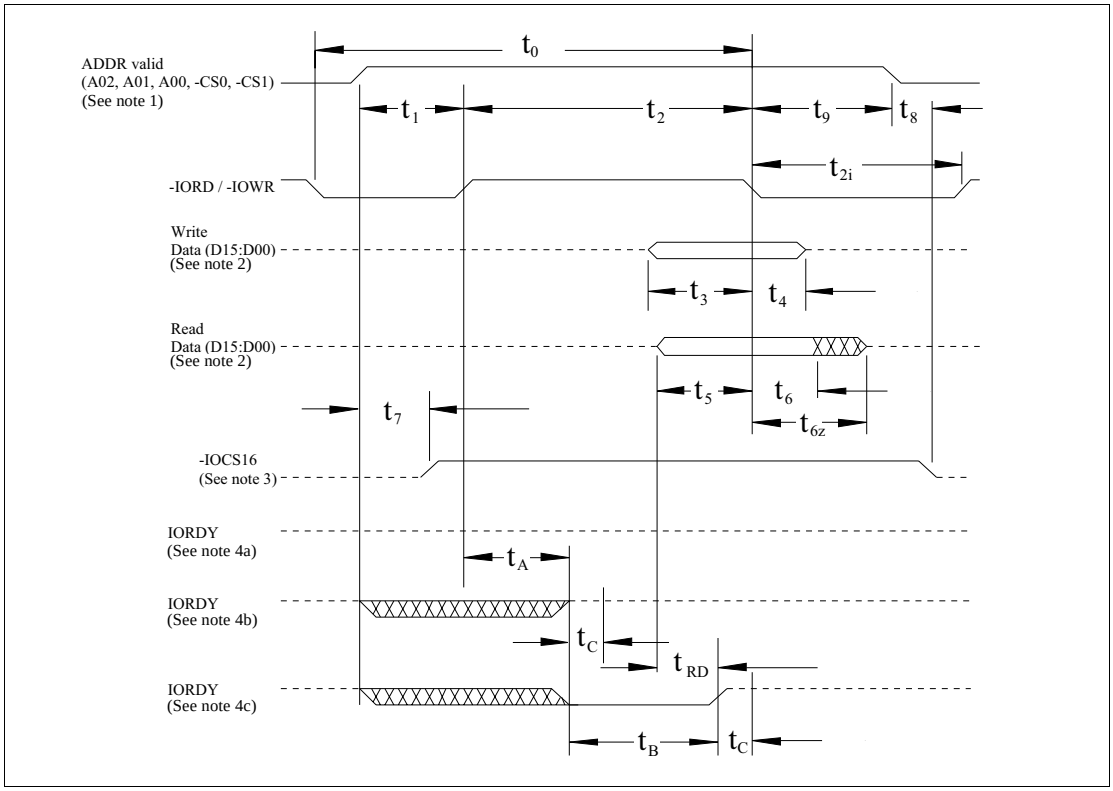

Figure 4: True IDE PIO Mode Read/Write Access Timing Diagram

Notes:

1. The device address consists of -CS0, -CS1, and A[02::00].
2. The data consists of D[15::00] (16-bit) or D[07::00] (8 bit).
3. -IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
   a. The device never negates IORDY; no wait is generated.
   b. The device starts to drive IORDY low before t_A, but causes IORDY to be asserted before t_A; no wait generated.
   c. The device drives IORDY low before t_A; wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device places read data on D15-D00 for t_{RD} before causing IORDY to be asserted.

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Table 11: True IDE PIO Mode Read/Write Access Timing

Symbol	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Note	Units
t_0	Cycle Time (minimum)	600	383	240	180	120	100	80	1	ns
t_1	Address Valid to IORD/-IOWR Setup (minimum)	70	50	30	30	25	15	10	-	ns
t_2	-IORD/-IOWR (minimum)	165	125	100	80	70	65	55	1	ns
t_2	-IORD/-IOWR (minimum) register (8 bit)	290	290	290	80	70	65	55	1	ns
t_{2i}	-IORD/-IOWR Recovery Time (minimum)	-	-	-	70	25	25	20	1	ns
t_3	-IOWR Data Setup (minimum)	60	45	30	30	20	20	15	-	ns
t_4	-IOWR Data Hold (minimum)	30	20	15	10	10	5	5	-	ns
t_5	-IORD Data Setup (minimum)	50	35	20	20	20	15	10	-	ns
t_6	-IORD Data Hold (minimum)	5	5	5	5	5	5	5	-	ns
t_{6Z}	-IORD Data Tristate (maximum)	30	30	30	30	30	20	20	2	ns
t_7	Address Valid to IOCS16 Assertion (maximum)	90	50	40	N/A	N/A	N/A	N/A	4	ns
t_8	Address Valid to IOCS16 Released (maximum)	60	45	30	N/A	N/A	N/A	N/A	4	ns
t_9	-IORD/-IOWR to Address Valid Hold	20	15	10	10	10	10	10	-	ns
t_{RD}	Read Data Valid to IORDY Active (minimum), if IORDY is initially low after t_A	0	0	0	0	0	0	0	-	ns
t_A	IORDY Setup Time	35	35	35	35	35	N/A[5]	N/A[5]	3	ns
t_B	IORDY Pulse Width (maximum)	1250	1250	1250	1250	1250	N/A[5]	N/A[5]	-	ns
t_C	IORDY Assertion to Release (maximum)	5	5	5	5	5	N/A[5]	N/A[5]	-	ns

Notes:

1. The symbol t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} must be met. The minimum total cycle time requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.
2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the Drive (tristate).

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3. The delay from the activation of -IORD or -IOWR until the state of IORDY is first sampled. If IORDY is inactive, then the host waits until IORDY is active before the PIO cycle can be completed. If the Drive is not driving IORDY negated at t_A after the activation of -IORD or -IOWR, then t_5 must be met and t_{RD} is not applicable. If the Drive is driving IORDY negated at the time t_A after the activation of -IORD or -IOWR, then t_{RD} must be met and t_5 is not applicable.
4. The symbols t_7 and t_8 apply only to modes 0, 1, and 2. For other modes, this signal is not valid.
5. IORDY is not supported in this mode.

True IDE PIO Multiword DMA Read/Write Access Timing

This function does not apply to SiliconDrive IIs that have DMA disabled.

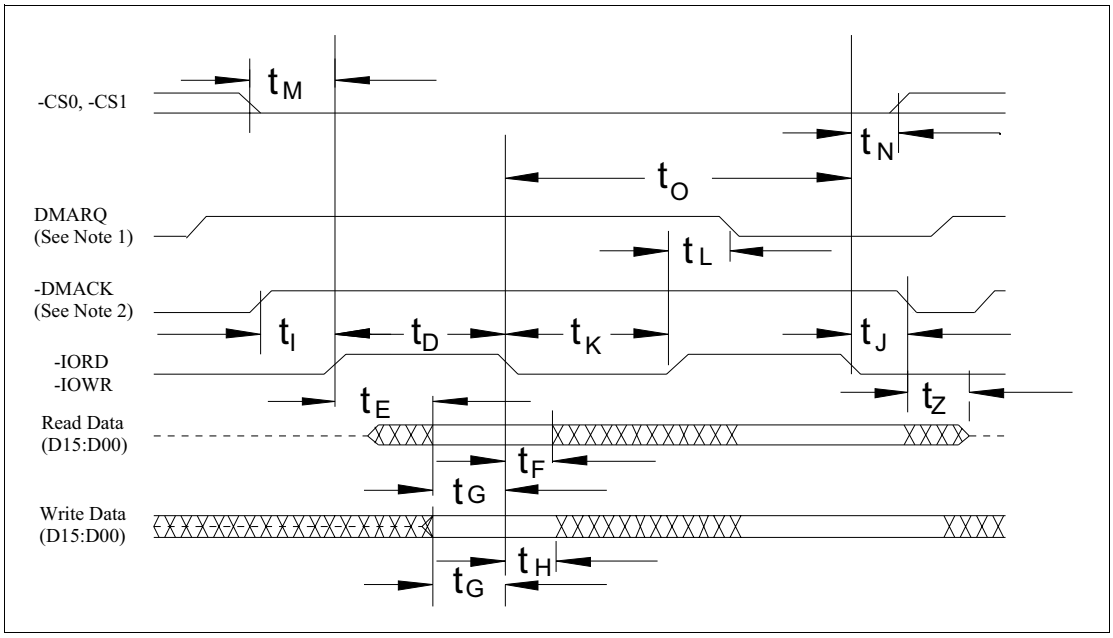

Figure 5: True IDE PIO Multiword DMA Read/Write Access Timing

Notes:

1. If the drive cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress, and reassert the signal at a later time to continue the DMA operation.
2. This signal may be negated by the host to suspend the DMA transfer in progress.

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Table 12: True IDE PIO Multiword DMA Read/Write Access Timing

Symbol	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note	Units
t_O	Cycle Time (minimum)	480	150	120	100	80	1	ns
t_D	-IORD/-IOWR Asserted Width (minimum)	215	80	70	65	55	1	ns
t_E	-IORD Data Access (maximum)	150	60	50	50	45	-	ns
t_F	-IORD Data Hold (minimum)	5	5	5	5	5	-	ns
t_G	-IORD/-IOWR Data Setup (minimum)	100	30	20	15	10	-	ns
t_H	-IOWR Data Hold (minimum)	20	15	10	5	5	-	ns
t_I	DMACK to –IORD/-IOWR Setup (minimum)	0	0	0	0	0	-	ns
t_J	-IORD / -IOWR to -DMACK Hold (minimum)	20	5	5	5	5	-	ns
t_{KR}	-IORD Negated Width (minimum)	50	50	25	25	20	1	ns
t_{KW}	-IOWR Negated Width (minimum)	215	50	25	25	20	1	ns
t_{LR}	-IORD to DMARQ Delay (maximum)	120	40	35	35	35	-	ns
t_{LW}	-IOWR to DMARQ Delay (maximum)	40	40	35	35	35	-	ns
t_M	CS(1:0) Valid to –IORD / -IOWR	50	30	25	10	5	-	ns
t_N	CS(1:0) Hold	15	10	10	10	10	-	ns
t_Z	-DMACK	20	25	25	25	25	-	ns

Note:

1. The symbol t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery times or command inactive times for input and output cycles, respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} must be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR}, or t_{KW} for input and output cycles, respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR} and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.

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Ultra DMA Data Burst Timing Requirements

The following figures and table describe the requirements for the Ultra DMA (UDMA) data burst timing.

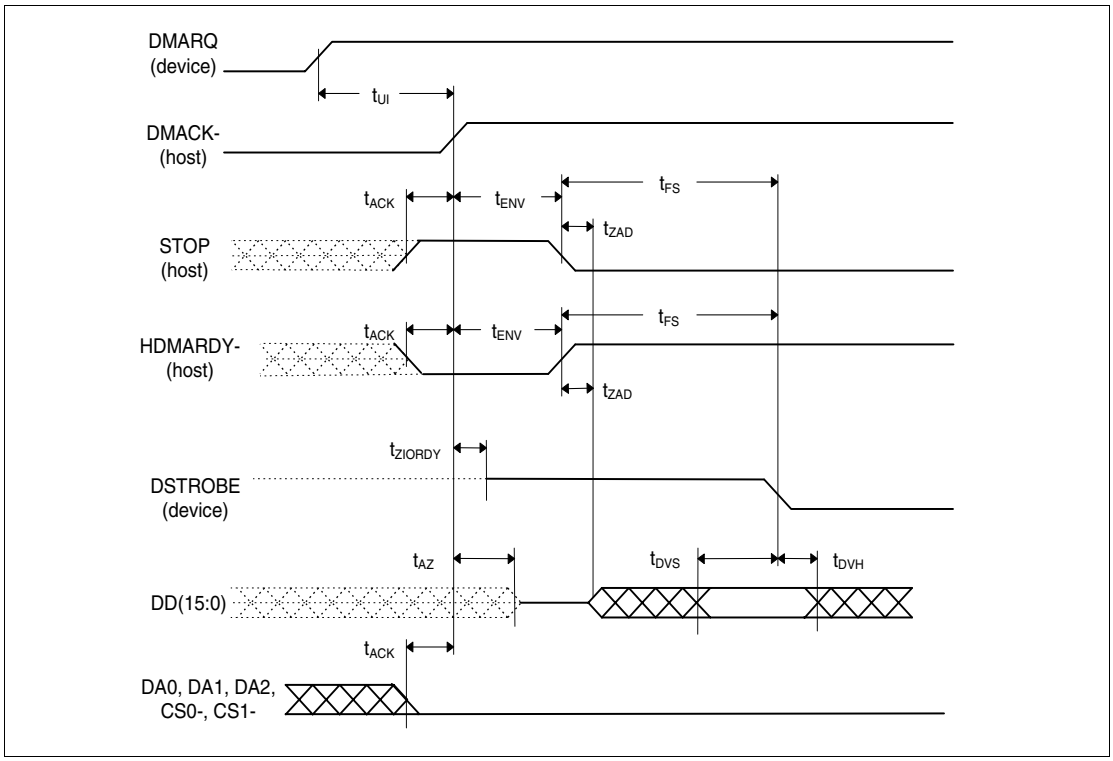

Figure 6: Initiating a UDMA Data-In Burst

Note: The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

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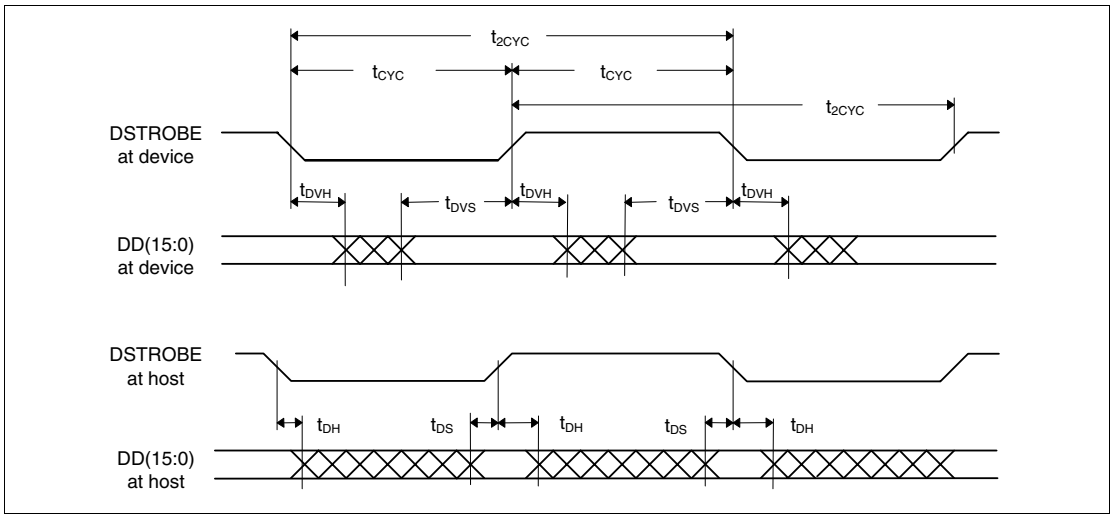

Figure 7: Sustained UDMA Data-In Burst

Note: DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that the cable settling time as well as cable propagation delay does not allow the data signals to be considered stable at the host until some time after they are driven by the device.

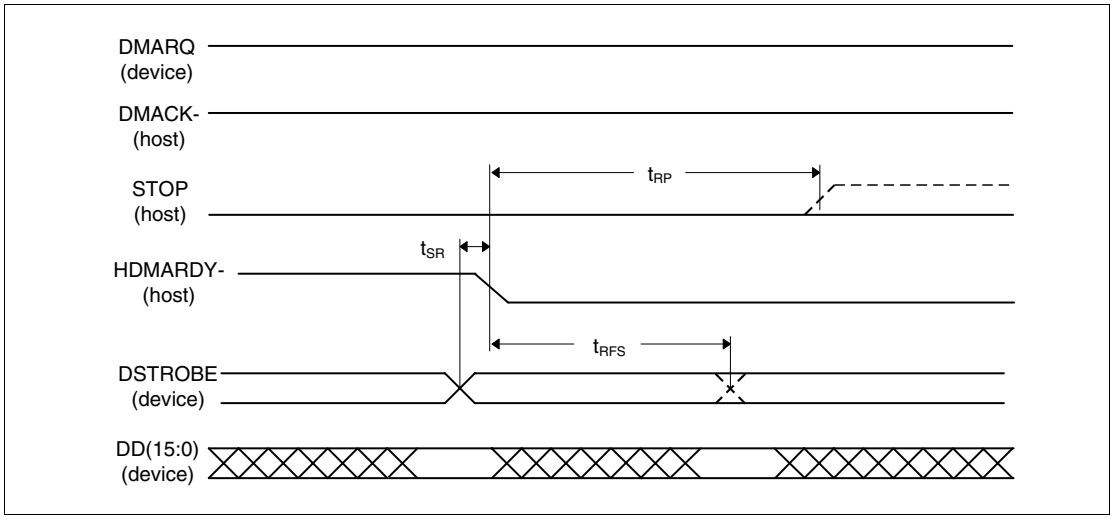

Figure 8: Host Pausing a UDMA Data-In Burst

Notes:

1. The host may assert STOP to request termination of the UDMA burst no sooner than t_{RP} after HDMARDY- is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the device.

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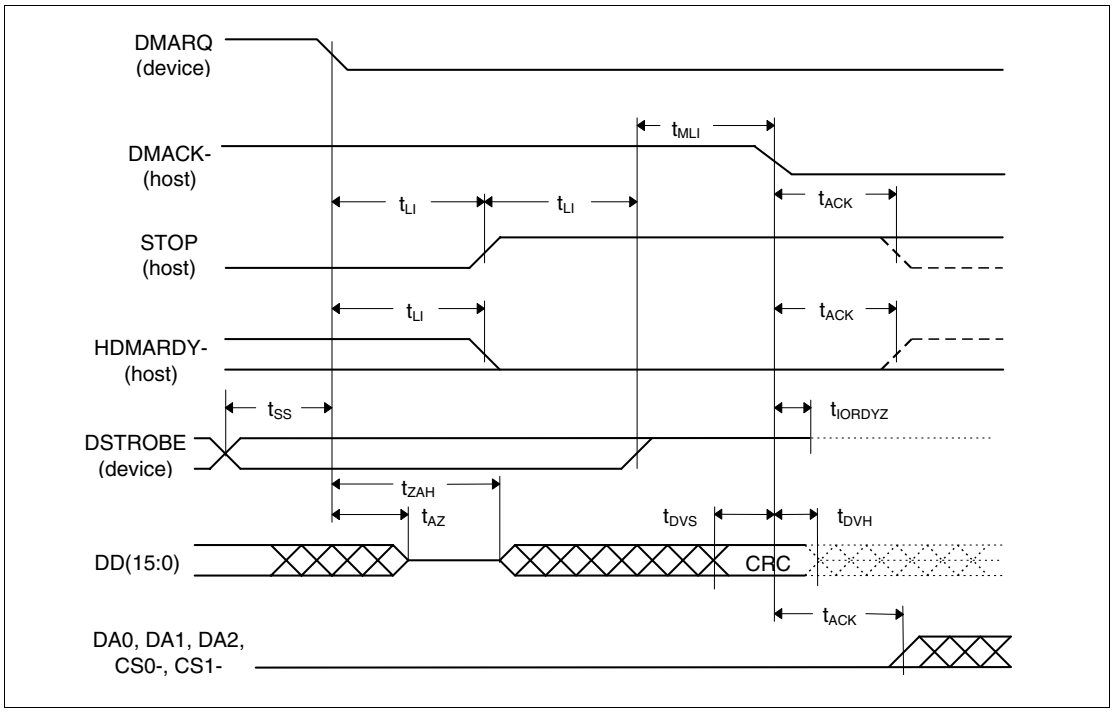

Figure 9: Device Terminating a UDMA Data-In Burst

Note: The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

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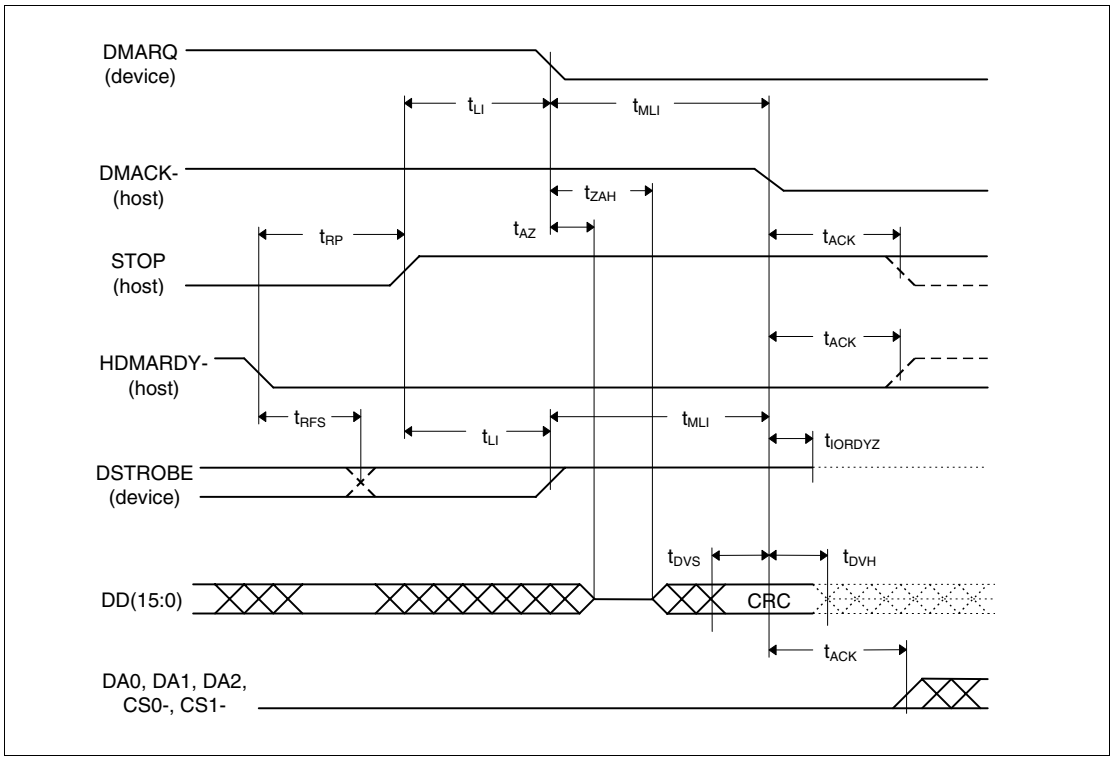

Figure 10: Host Terminating a UDMA Data-In Burst

Note: The definitions for the DIOW-:STOP, DIOR-:HDMARDY-:HSTROBE, and IORDY:DDMARDY-:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

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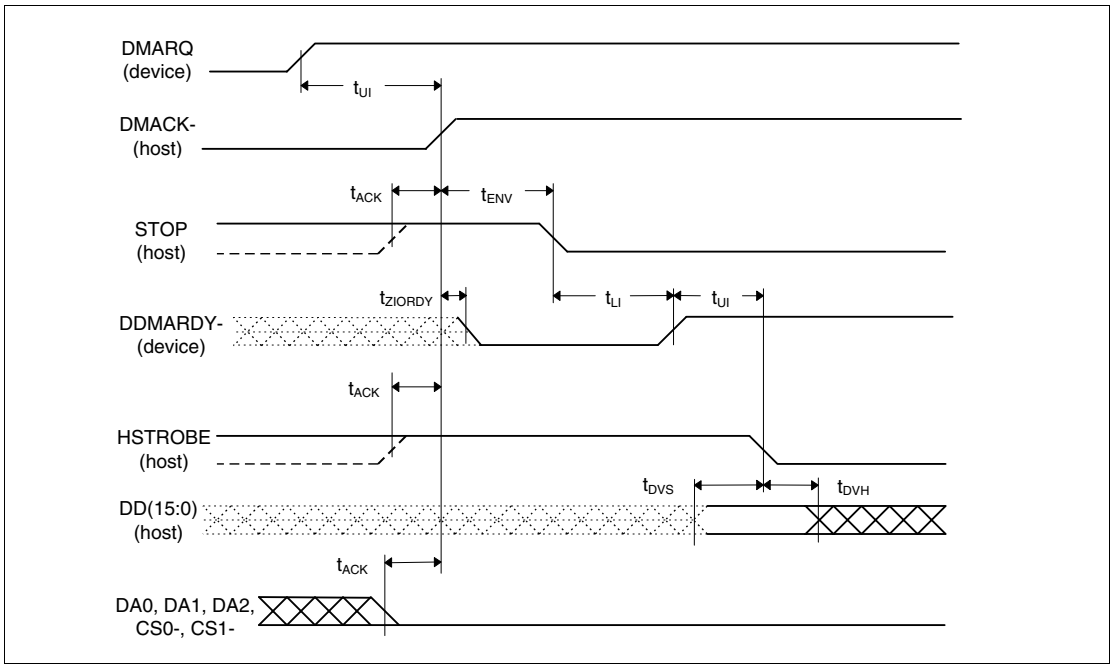

Figure 11: Initiating a UDMA Data-Out Burst

Note: The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

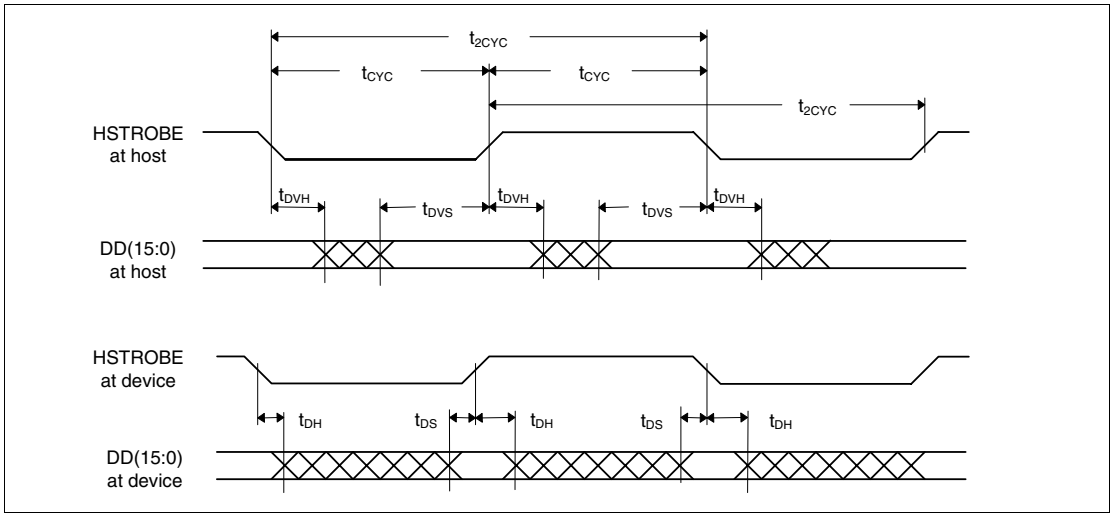

Figure 12: Sustained UDMA Data-Out Burst

Note: DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that the cable settling time as well as cable propagation delay does not allow the data signals to be considered stable at the device until some time after they are driven by the host.

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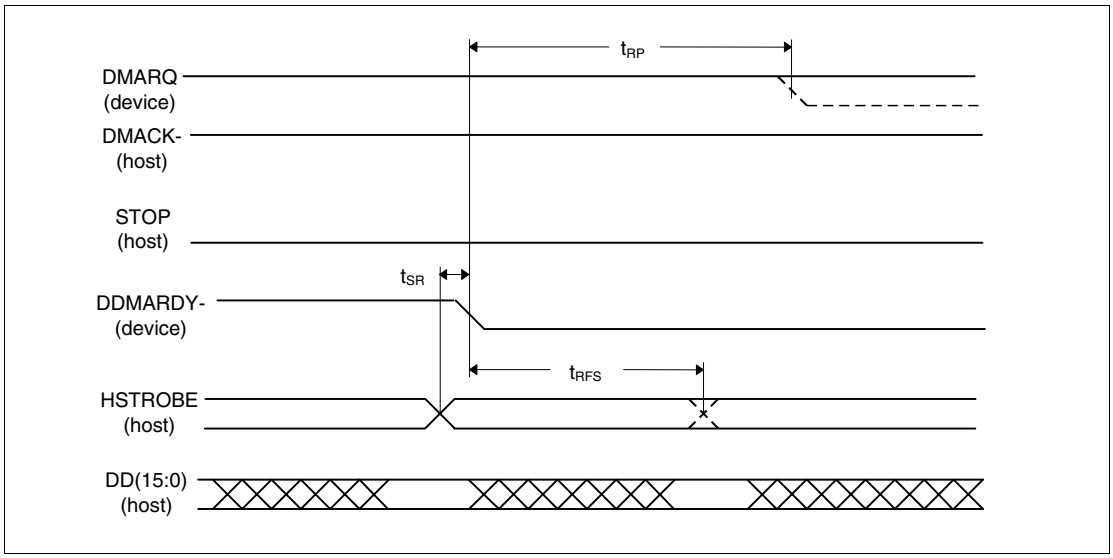

Figure 13: Device Pausing a UDMA Data-Out Burst

Notes:

1. The device may negate DMARQ to request termination of the UDMA burst no sooner than t_{RP} after DDMARDY- is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the host.

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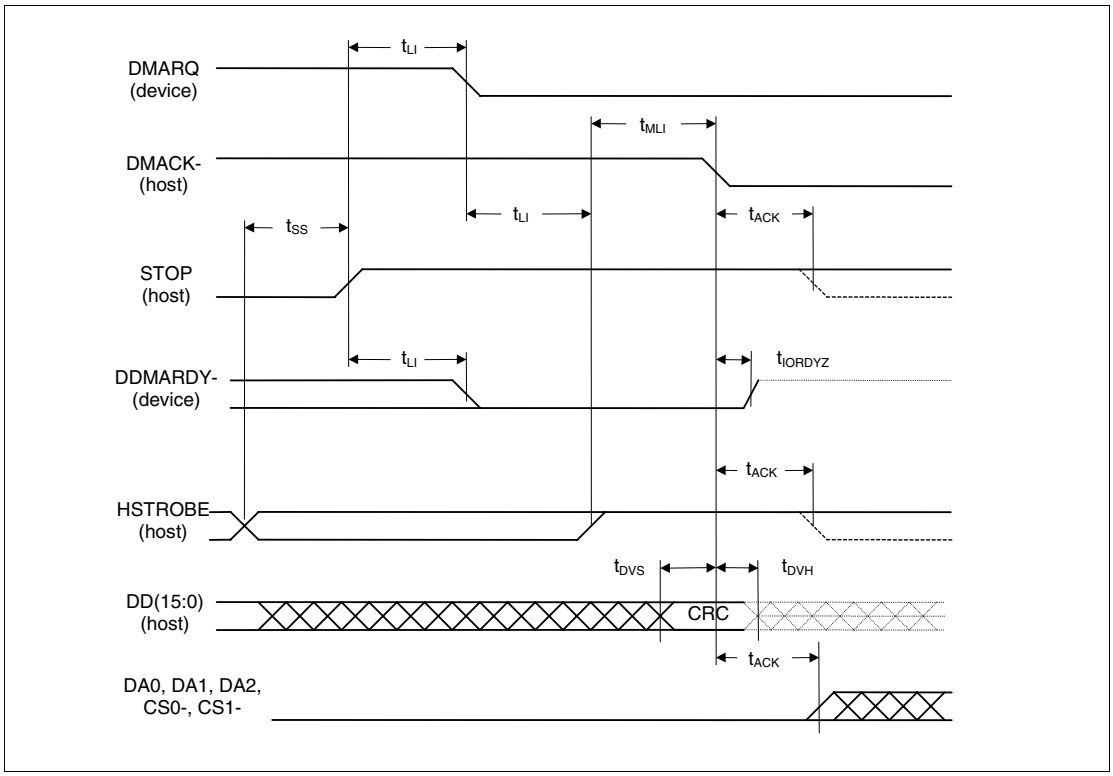

Figure 14: Host Terminating a UDMA Data-Out Burst

Note: The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

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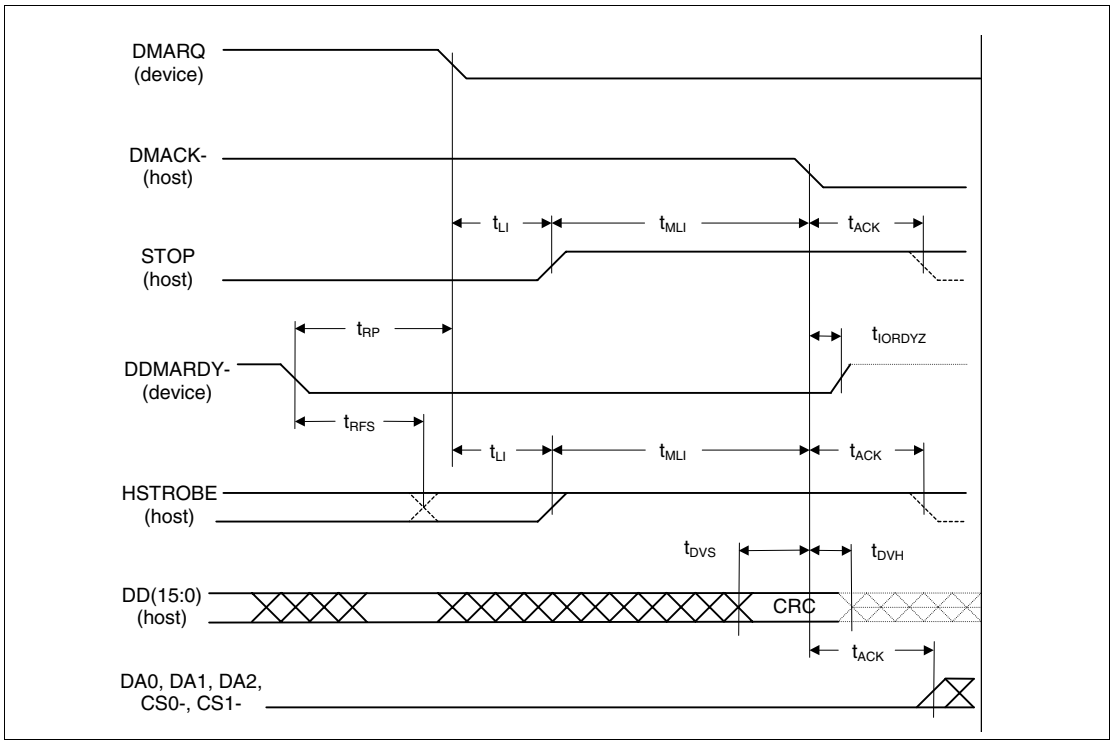

Figure 15: Device Terminating a UDMA Data-Out Burst

Note: The definitions for the DIOW-:STOP, IORDY:DDMARDY-:DSTROBE, and DIOR-:HDMARDY-:HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Table 13: UDMA Data Burst Timing Requirements

Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Comment (see Notes 1 and 2)	Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{2CYCTYP}$	240	-	160	-	120	-	90	-	60	-	Typical sustained average two-cycle time.	ns
t_{CYC}	112	-	73	-	54	-	39	-	25	-	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge).	ns
t_{2CYC}	230	-	154	-	115	-	86	-	57	-	Two-cycle time allowing for clock variations (from rising edge to next rising edge, or from falling edge to next falling edge of STROBE).	ns
t_{DS}	15		10		7		7		5		Data setup time at recipient.	ns
t_{DH}	5	-	5	-	5	-	5	-	5	-	Data hold time at recipient.	ns

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Table 13: UDMA Data Burst Timing Requirements (Continued)

Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Comment (see Notes 1 and 2)	Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{DVS}	70	-	48	-	30	-	20	-	6	-	Data valid setup time at sender (from data valid until STROBE edge) (see Note 4).	ns
t_{DVH}	6	-	6	-	6	-	6	-	6	-	Data valid hold time at sender (from STROBE edge until data may become invalid) (see Note 4).	ns
t_{FS}	0	230	0	200	0	170	0	130	0	120	First STROBE time (for device to first negate DSTROBE from STOP during a data-in burst).	ns
t_{LI}	0	150	0	150	0	150	0	100	0	100	Limited interlock time (see Note 3).	ns
t_{MLI}	20	-	20	-	20	-	20	-	20	-	Interlock time with minimum (see Note 3).	ns
t_{UI}	0	-	0	-	0	-	0	-	0	-	Unlimited interlock time (see Note 3).	ns
t_{AZ}	-	10	-	10	-	10	-	10	-	10	Maximum time allowed for output drivers to release (from asserted or negated).	ns
t_{ZAH}	20	-	20	-	20	-	20	-	20	-	Minimum delay time required for output.	ns
t_{ZAD}	0	-	0	-	0	-	0	-	0	-	Drivers to assert or negate (from released).	ns
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Envelope time (from DMACK- to STOP and HDMARDY- during data-in burst initiation, and from DMACK to STOP during data-out burst initiation).	ns
t_{SR}	-	50	-	30	-	20	-	NA	-	NA	STROBE to DMARDY- time (if DMARDY- is negated before this long after STROBE edge, the recipient receives no more than one additional data word).	ns
t_{RFS}	-	75	-	70	-	60	-	60	-	60	Ready-to-final STROBE time (no STROBE edges are sent this long after negation of DMARDY-).	ns
t_{RP}	160	-	125	-	100	-	100		100	-	Minimum time to assert STOP or negate DMARQ.	ns
t_{IORDYZ}	-	20	-	20	-	20	-	20	-	20	Maximum time before releasing IORDY.	ns
t_{ZIORDY}	0	-	0	-	0	-	0	-	0	-	Minimum time before driving STROBE (see note 5).	ns
t_{ACK}	20	-	20	-	20	-	20	-	20	-	Setup and hold times for DMACK- (before assertion or negation).	ns

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Table 13: UDMA Data Burst Timing Requirements (Continued)

Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Comment (see Notes 1 and 2)	Units
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{SS}	50	-	50	-	50	-	50	-	50	-	Time from STROBE edge to negation of DMARQ or assertion of STOP (when the sender terminates a burst).	ns

Notes:

1. Timing parameters are measured at the connector of the sender or receiver to which the parameter applies. Both STROBE and DMARDY- timing measurements are taken at the sender's connector.

   Example: For example, the sender stops generating STROBE edges t_{RFS} after the negation of DMARDY-.

2. All timing measurement switching points (low-to-high and high-to-low) are taken at 1.5V.
3. The symbols t_{UI}, t_{MLI}, and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks (i.e., either the sender or recipient is waiting for the other to respond with a signal before proceeding). The symbol t_{UI} is an unlimited interlock that has no maximum time value, t_{MLI} is a limited time-out that has a defined minimum, and t_{LI} is a limited time-out that has a defined maximum.
4. The test load for t_{DVS} and t_{DVH} are a lumped capacitor load with no cable or receivers. Timing for t_{DVS} and t_{DVH} are met for all capacitive loads from 15pF to 40pF where all signals have the same capacitive load value.
5. The symbol t_{ZIORDY} may be greater than t_{ENV} since the device has a pull-up on IORDY- giving it a known state when released.

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ATA AND TRUE IDE REGISTER DECODING

SiliconDrive II can be configured as either a a memory-mapped or an an I/O devices. As noted earlier, communication to and from the drive is accomplished using the ATA Command Block.

TASK FILE REGISTER SPECIFICATION

The Task File registers are used for reading and writing the storage data in the SiliconDrive II. The decoded addresses are as shown in the following table.

Table 14: Task File Register Specification

CS0#	CS1#	DA02	DA01	DA00	DIOR# = L	DIOW# = L
0	1	0	0	0	Data	Data
0	1	0	0	1	Error	Feature
0	1	0	1	0	Sector Count	Sector Count
0	1	0	1	1	Sector Number	Sector Number
0	1	1	0	0	Cylinder Low	Cylinder Low
0	1	1	0	1	Cylinder High	Cylinder High
0	1	1	1	0	Drive/Head	Drive/Head
0	1	1	1	1	Status	Command
0	0	X	X	X	Invalid	Invalid
1	1	X	X	X	High-Z	Not Used
1	0	0	X	X	High-Z	Not Used
1	0	1	0	X	High-Z	Not Used
1	0	1	1	0	Alternate Status	Device Control
1	0	1	1	1	Device Address	Not Used

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ATA REGISTERS

DATA REGISTER

The Data register is a 16-bit register used to transfer data blocks between the host and drive buffers. The register may set to 8-bit mode by using the Set Features Command defined in "Seek — 7Xh" on page 59.

ERROR REGISTER

The Error register contains the error status, if any, generated from the last executed ATA command. The contents are qualified by the ERR bit being set in "Status Register" on page 35.

Table 15: Error Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read	BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	**Bad Block Detected (BBK).** Set when a bad block is detected.
6	**Uncorrectable Data Error (UNC).** Set when an uncorrectable error is encountered.
5	**Media Changed (MC).** Set to 0.
4	**ID Not Found (IDNF).** Set when the sector ID is not found.
3	**MCR (Media Change Request).** Set to 0.
2	**Aborted Command (ABRT).** Set when a command is aborted due to a drive error.
1	**Track 0 Not Found (TKONF).** Set when the execute drive diagnostic command is executed.
0	**Address Mark Not Found (AMNF).** Set in the case of a general error.

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FEATURE REGISTER

The Feature register is command-specific and used to enable and disable interface features. This register supports only either odd or even byte data transfers.

Table 16: Feature Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Feature Byte							

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SECTOR COUNT REGISTER

The Sector Count register is used to read or write the sector count of the data for which an ATA transfer has been made.

Table 17: Sector Count Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Count							
Default Value	0	0	0	0	0	0	0	1

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SECTOR NUMBER REGISTER

The Sector Number register is set by the host to specify the starting sector number associated with the next ATA command to be executed. Following a qualified ATA command sequence, the device sets the register value to the last sector read or written as a result of the previous AT command.

When Logical Block Addressing (LBA) mode is implemented and the host issues a command, the contents of the register describe the Logical Block Number bits A[7:0]. Following an ATA command, the device loads the register with the LBA block number resulting from the last ATA command.

Table 18: Sector Number Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Sector Number (CHS Addressing)							
	Logical Block Number bits A07-A00 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	1

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CYLINDER LOW REGISTER

The Cylinder Low register is set by the host to specify the cylinder number low byte. Following an ATA command, the content of the register is written by the device, identifying the cylinder number low byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A15:A08.

Table 19: Cylinder Low Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A15-A08 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

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CYLINDER HIGH REGISTER

The Cylinder High register is set by the host to specify the cylinder number high byte. Following an ATA command, the content of the register is set internally by the device, identifying the cylinder number high byte.

In LBA mode, the 8-bit register maintains the contents of the Logical Block number address bits A23:A16.

Table 20: Cylinder High Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	Cylinder Number Low Byte (CHS Addressing)							
	Logical Block Number bits A23-A16 (LBA Addressing)							
Default Value	0	0	0	0	0	0	0	0

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DRIVE/HEAD REGISTER

The Drive/Head register is used by the host and the device to select the type of addressing (CHS or LBA), the drive letter, and either bits 3-0 of the head number in CHS mode or logical block number bits 27-24 in LBA mode.

Table 21: Drive/Head Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	1	LBA	1	DRV	HS3 LBA27	HS2 LBA26	HS1 LBA25	HS0 LBA24
Default Value	1	0	1	0	0	0	0	0

The Drive/Head register is used by the host to specify one of a pair of ATA drives present in the platform.

Bit(s)	Description
6	**LBA.** Selects between CHS (0) and LBA (1) addressing mode.
4	**Drive Address (DRV).** Indicates the drive number selected by the host, either 0 or 1.
3-0	HS3 to 0. Indicates bits 3-0 of the head number in CHS addressing mode or LBA bits 27-24 in LBA mode. • CHS to LBA conversion: LBA = (C x HpC + H) x SpH + S -1 • LBA to CHS conversion: ◦ C = LBA/(HpC x SpH) ◦ H = (LBA/SpH) mod (HpC) ◦ S = (LBA mod(SpH)) + 1 ...where: ◦ C is the cylinder number ◦ H is the head number ◦ S is the sector count ◦ HpC is the head count per cylinder count ◦ SpH is the sector count per head count (track)

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STATUS REGISTER

The Status register provides the device's current status to the host. The status register is an 8-bit read-only register. When the contents of the register are read by the host, the IREQ# bit is cleared.

Table 22: Status Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

Bit(s)	Description
7	**Busy (BSY).** Set when the drive is busy and unable to process any new ATA commands.
6	**Data Ready (DRDY).** Set when the device is ready to accept ATA commands from the host.
5	**Drive Write Fault (DWF).** Always set to 0.
4	**Drive Seek Complete (DSC).** Set when the drive heads have been positioned over a specific track.
3	**Data Request (DRQ).** Set when a device is ready to transfer a word or byte of data to or from the host and the device.
2	**Corrected Data (CORR).** Always set to 0.
1	**Index (IDX).** Always set to 0.
0	**Error (ERR).** Set when an error occurs during the previous ATA command.

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COMMAND REGISTER

The Command register specifies the ATA command code being issued to the drive by the host. Execution of the command begins immediately following the issuance of the command register code by the host.

Table 23: Command Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	ATA Command Code							

See "All but CU / E / MU / R / SD/MMC+:ATA Command Block and Set Description" on page 120 for a listing of the supported ATA commands.

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ALTERNATE STATUS REGISTER

The Alternate Status register is a read-only register indicating the status of the device, following the previous ATA command. See "Status Register" on page 35 for specific details.

Table 24: Alternate Status Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
Default Value	0	0	0	0	0	0	0	0

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DEVICE CONTROL REGISTER

The Device Control register is used to control the interrupt request and issue ATA software resets.

Table 25: Device Control Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Write	-	-	-	-	1	SRST	nIEN	0

Bit(s)	Description
7-4	Reserved bits.
3	Always set to 1.
2	**Software Reset (SRST).** When set, resets the ATA software.
1	**Interrupt Enable (nIEN).** When set, device interrupts are disabled. There is no function in the memory-mapped mode.
0	Always set to 0.

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DEVICE ADDRESS REGISTER

The Device Address register is used to maintain compatibility with ATA disk drive interfaces.

Table 26: Device Address Register

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Read/Write	-	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0
Default Value	0	0	1	1	1	1	1	0

Bit(s)	Description
7	Reserved bit.
6	**Write Gate (nWTG).** Low when a write to the device is in process.
5-2	**nHS3 to nHS0.** The negated binary address of the currently selected head.
1	**nDS1.** Low when drive 1 is selected and active.
0	**nDS0.** Low when drive 0 is selected and active.

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ATA COMMAND BLOCK AND SET DESCRIPTION

In accordance with the *ANSI ATA Specification*, the device implements seven registers that are used to transfer instructions to the device by the host. These commands follow the ANSI standard ATA protocol. A description of the ATA command block is provided in the following table.

Table 27: ATA Command Block and Set Description

Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	X							

ATA COMMAND SET

Table 28: ATA Command Set

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98h, E5h	-	-	-	-	D	-
1	Execute Drive Diagnostics	90h	-	-	-	-	D	-
1	Erase Sector	C0h	-	Y	Y	Y	Y	Y
2	Format Track	50h	-	Y	-	Y	Y	Y
1	Identify Drive	ECh	-	-	-	-	D	-
1	Idle	97h, E3h	-	Y	-	-	D	-
1	Idle Immediate	95h, E1h	-		-	-	D	-
1	Initialize Drive Parameters	91h	-	Y	-	-	Y	-
1	Read Buffer	E4h	-	-	-	-	D	-
1	Read DMA*	C8h	-	Y	Y	Y	Y	Y
1	Read Multiple	C4h	-	Y	Y	Y	Y	Y

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Table 28: ATA Command Set (Continued)

Class	Command Name	Command Code	Registers Used					
			FR	SC	SN	CY	DH	LBA
1	Read Long Sector	22h, 23h	-	-	Y	Y	Y	Y
1	Read Sector(s)	20h, 21h	-	-	Y	Y	Y	Y
1	Read Verify Sector(s)	40h, 41h	-	Y	Y	Y	Y	Y
1	Recalibrate	1Xh	-	-	-	-	Y	-
1	Request Sense	03h	-	-	-	-	D	-
1	Seek	7Xh	-	-	Y	Y	Y	Y
1	Set Features	EFh	Y		-	-	D	-
1	Set Multiple Mode	C6h	-	Y	-	-	D	-
1	Set Sleep Mode	99h, E6h	-	-	-	-	D	-
1	Standby	96h, E2h	-	-	-	-	D	-
1	Standby Immediate	94h, E0h	-	-	-	-	D	-
1	Translate Sector	87h	-	Y	Y	Y	Y	Y
1	Wear Level	F5h	-	-	-	-	Y	-
2	Write Buffer	E8h	-	-	-	-	D	-
1	Write DMA*	CAh	-	Y	Y	Y	Y	Y
2	Write Long Sector	32h, 33h	-		Y	Y	Y	Y
3	Write Multiple	C5h	-	Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30h, 31h	-	Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
3	Write Verify	3Ch	-	Y	Y	Y	Y	Y

* = This function does not apply to SiliconDrive IIs that have DMA disabled.

Notes:

- CY = Cylinder
- SC = Sector Count
- DH = Drive/Head
- SN = Sector Number
- FR = Feature LBA — LBA bit of the Drive/Head register (D denotes that only the drive bit is used)

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Check Power Mode — 98h, E5h

The Check Power Mode command verifies the device's current power mode. When the device is configured for standby mode or is entering or exiting standby, the BSY bit is set, the Sector Count register set to 00h, and the BSY bit is cleared. In idle mode, BSY is set and the Sector Count register is set to FFh. The BSY bit is then cleared and an interrupt is issued.

Table 29: Check Power Mode — 98h, E5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	98h or E5h							

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Executive Drive Diagnostic — 90h

The Executive Drive Diagnostic performs an internal read write diagnostic test using (AA55h and 55AAh). If an error is detected in the read/write buffer, the Error register reports the appropriate diagnostic code.

Table 30: Executive Drive Diagnostic — 90h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive				
Command	90h							

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Format Track — 50h

The Format Track command formats the common solid-state memory array.

Table 31: Format Track — 50h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	50h							

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Identify Drive — ECh

Issued by the host, the Identify Drive command provides 256 bytes of drive attribute data (i.e., sector size, count, and so on) The identify drive data structure is detailed in the following table.

Table 32: Identify Drive — ECh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	ECh							

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Identify Drive — Drive Attribute Data

Table 33: Identify Drive — Drive Attribute Data

Word Address	Data Default	Bytes	Data Description
0	045Ah	2	General configuration bit information • 15: Non-magnetic disk • 14: Formatting speed latency permissible gap needed • 13: Track Offset option supported • 12: Data Strobe Offset option supported • 11: Over 0.5% rotational speed difference • 10: Disk transfer rate > 10Mbps • 9: 10Mbps >= disk transfer rate > 5Mbps • 8: 5Mbps >= disk transfer rate • 7: Removable cartridge drive • 6: Fixed drive • 5: Spindle Motor Control option executed • 4: Over 15µs changing head time • 3: Non-MFM encoding • 2: Soft sector allocation • 1: Hard sector allocation • 0: Reserved
1	XXXXh	2	Number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Number of heads
4	0000h	2	Number of unformatted bytes per track
5	XXXXh	2	Number of unformatted bytes per sector
6	XXXXh	2	Number of sectors per track
7-8	XXXXh	4	Number of sectors per device
9	0000h	2	Reserved
10-19	XXXXh	20	Serial number

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Table 33: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
20	0001h	2	Buffer type • 0000h: Not specified • 0001h: A single-ported, single-sector buffer • 0002h: A dual-ported multisector buffer • 0003h: A dual-ported multisector buffer with a read caching
21	0001h	2	Buffer size in 512-byte increments
22	0004h	2	Number of ECC bytes passed on read/ write long commands
23-26	XXXXh	8	Firmware revision (eight ASCII characters)
27-46	XXXXh	40	Model number (40 ASCII characters)
47	8001h	2	15-8: Maximum number of sectors that can be transferred with a Read/Write Multiple command per interrupt
48	0000h	2	Double word (32 bit) not supported
49	0f00h	2	• 11: IORDY supported • 9: LBA supported • 8: DMA supported
50	0000h	2	Reserved
51	0200h	2	15-8: PIO data transfer cycle timing
52	0000h	2	15-8: DMA data transfer cycle timing
53	0007h	2	• 2: Word 88 is valid • 1: Words 64-70 are valid • 0: Words 54-58 are valid
54	XXXXh	2	Current number of cylinders
55	XXXXh	2	Current number of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors
59	010Xh	2	7-0: Current sectors can be transferred with a Read/Write Multiple command per interrupt
60-61	XXXXh	4	Total number of sectors addressable in LBA mode

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Table 33: Identify Drive — Drive Attribute Data (Continued)

Word Address	Data Default	Bytes	Data Description
62	0000h	2	Single-word DMA modes supported
63	0007h	2	• 2: Multiword DMA mode 2 supported • 1: Multiword DMA mode 1 supported • 0: Multiword DMA mode 0 supported
64	0003h	2	7-0: Advanced PIO modes supported
65	0078h	2	15-0: Multiword DMA cycle time in nanoseconds
66	0078h	2	15-0: Multiword DMA transfer cycle time in nanoseconds
67	0078h	2	15-0: PIO mode cycle time without flow control
68	0078h	2	15-0: PIO mode cycle time with IORDY flow control
80	003Eh	2	• 5: ATA/ATAPI-5 supported • 4: ATA/ATAPI-4 supported • 3: ATA-3 supported • 2: ATA-2 supported • 1: ATA-2 supported • 0: Reserved
88	001Fh	2	• 4: UDMA mode 4 supported • 3: UDMA mode 3 supported • 2: UDMA mode 2 supported • 1: UDMA mode 1 supported • 0: UDMA mode 0 supported
163	0002h	2	2: Multiword DMA mode 2 and PIO mode 6 supported

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Idle — 97h, E3h

When issued by the host, the device's internal controller sets the BSY bit, enters the Idle mode, clears the BSY bit, and generates an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5ms, and the automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is disabled.

Table 34: Idle — 97h, E3h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count (5ms increments)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	97h or E3h							

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Idle Immediate — 95h, E1h

When issued by the host, the device's internal controller sets the BSY bit, enters Idle Mode, clears the BSY bit, and issues an interrupt. The interrupt is issued whether or not the Idle mode is fully entered.

Table 35: Idle Immediate — 95h, E1h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	95h or E1h							

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Initialize Drive Parameters — 91h

Initialize Drive Parameters allows the host to set the sector counts per track and the head counts per cylinder to 1 Fixed. Upon issuance of the command, the device sets the BSY bit and associated parameters, clears the BSY bit, and issues an interrupt.

Table 36: Initialize Drive Parameters — 91h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count (Number of Sectors)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	0	X	Drive	Head Number (Number of Heads — 1)			
Command	91h							

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Recalibrate — 1Xh

The Recalibrate command sets the cylinder low and high, head number to 0h, and sector number to 1h in CHS mode. In LBA mode (i.e., LBA = 1), the sector number is set to 0h.

Table 37: Recalibrate — 1Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	LBA	1	Drive	X			
Command	1Xh							

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Read Buffer — E4h

The Read Buffer command allows the host to read the contents of the sector buffer. When issued, the device sets the BSY bit and sets up the sector buffer data in preparation for the read operation. When the data is ready, the DRQ bit is set and the BSY bit in the Status register are set and cleared, respectively.

Table 38: Read Buffer — E4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E4h							

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Read DMA — C8h

The Read DMA command allows the host to read data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrive IIs that have DMA disabled.

Table 39: Read DMA — C8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C8h							

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Read Multiple — C4h

The Read Multiple command executes similarly to the Read Sector command, with the exception that interrupts are issued only when a block containing the counts of sectors defined by the Set Multiple command is transferred.

Table 40: Read Multiple — C4h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	C4h							

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Read Sector — 20h, 21h

The Read Sector command allows the host to read sectors 1 to 256 as specified in the Sector Count register. If the sector count is set to 0h, all 256 sectors of data are made available. When the command code is issued and the first sector of data has been transferred to the buffer, the DRQ bit is set. The Read Sector command is terminated by writing the cylinder, head, and sector number of the last sector read in the task file. On error, the read operation is aborted in the errant sector.

Table 41: Read Sector — 20h, 21h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	20h or 21h							

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Read Long Sector(s) — 22h, 23h

The Read Long Sector(s) command operates similarly to the Read Sector(s) command, with the exception that it transfers requested data sectors and ECC data. The long instruction ECC byte transfer for Long commands is a byte transfer at a fixed length of 4 bytes.

Table 42: Read Long Sector(s) — 22h, 23h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	22h or 23h							

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Read Verify Sector(s) — 40h, 41h

The Read Verify Sector(s) command operates similarly to the Read Sector(s) command, with the exception that is does not set the DRQ bit and does not transfer data to the host. When the requested sectors are verified, the onboard controller clears the BSY bit and issues an interrupt.

Table 43: Read Verify Sector(s) — 40h, 41h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	40h or 41h							

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Seek — 7Xh

The Seek command seeks and picks up the head to the tracks specified in the task file. When the command is issued, the solid-state memory chips do not need to be formatted. After an appropriate amount of time, the DSC bit is set.

Table 44: Seek — 7Xh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	7Xh							

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Set Features — EFh

The Set Features command allows the host to configure the feature set of the device according to the attributes listed in Table 46.

Table 45: Set Features — EFh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	Feature							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	EFh							

Table 46: Set Features' Attributes

Feature	Operation
01h	Enable 8-bit data transfer
66h	Disable reverting to power on defaults
81h	Disable 8-bit data transfer
BBh	4 bytes of data apply on Read/Write Long commands
CCh	Enable revert to power on defaults

On power-up or following a hardware reset, the device is set to the default mode 81h.

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Set Multiple Mode — C6h

The Set Multiple Mode command allows the host to access the drive via Read Multiple and Write Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple command. The sector count per block is set in the Sector Count register.

Table 47: Set Multiple Mode — C6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	C6h							

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Set Sleep Mode — 99h, E6h

The Set Sleep Mode command allows the host to set the device in sleep mode. When the onboard controller transitions to sleep mode, it clears the BSY bit and issues an interrupt. The device interface then becomes inactive. Sleep mode can be exited by issuing either a hardware or software reset.

Table 48: Set Sleep Mode — 99h, E6h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	99h or E6h							

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Standby — 96h, E2h

When the Standby command is issued by the host, it transitions the device into standby mode. If the Sector Count register is set to a value other than 0h, the Auto Powerdown function is enabled and the device returns to Idle mode.

Table 49: Standby — 96h, E2h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Timer Count (5ms x Timer Count)							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	96h or E2h							

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Standby Immediate — 94h, E0h

When the Standby Immediate command is issued by the host, it transitions the device into standby mode.

Table 50: Standby Immediate — 94h, E0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_7
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	94h or E0h							

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Write Buffer — E8h

The Write Buffer command allows the host to rewrite the contents of the 512- byte data buffer with the wanted data.

Table 51: Write Buffer — E8h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_7
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	X			
Command	E8h							

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Write DMA — CAh

The Write DMA command allows the host to write data using the DMA transfer protocol.

Note: This function does not apply to SiliconDrive IIs that have DMA disabled.

Table 52: Write DMA — CAh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	CAh							

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Write Multiple — C5h

The Write Multiple command operates in the same manner as the Write Sector command. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 53: Write Multiple — C5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low(LBA15-8)							
Cylinder High	Cylinder High(LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number(LBA27-24)			
Command	C5h							

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Write Sector(s) — 30h, 31h

The Write Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. When issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 54: Write Sector(s) — 30h, 31h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	30h or 31h							

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Write Long Sector(s) — 32h, 33h

The Write Long Sector(s) command operates in the same manner as the Write Sector command — when issued, the device sets the BSY bit within 400ns and generates an interrupt at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

Table 55: Write Long Sector(s) — 32h, 33h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	32h or 33h							

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Erase Sector(s) — C0h

The Erase Sector(s) command is issued prior to the issuance of a Write Sector(s) or Write Multiple w/o Erase command.

Table 56: Erase Sector(s) — C0h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	C0h							

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Request Sense — 03h

The Request Sense command identifies the extended error codes generated by the preceding ATA command. The Request Sense command must be issued immediately following the detection of an error via the Error register.

Table 57: Request Sense — 03h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	X							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	1	X	1	Drive	X			
Command	03h							

The extended error codes are defined in the following table.

Table 58: Extended Error Codes

Extended Error Codes	Description
00h	No error detected
01h	Self test is OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (requested head or sector invalid)
2Fh	Address overflow (address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30h-32h, 37h,3Eh	Self test of diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Computed media format
03h	Write/erase failed

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Translate Sector — 87h

The Translate Sector command is not currently supported by the SiliconSystems' SiliconDrive II. If the host issues this command, the device responds with 0x00h in the data register.

Table 59: Translate Sector — 87h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	1	LBA	1	Drive	Head Number (LBA27-24)			
Command	87h							

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Wear-Level — F5h

The Wear-Level command is supported as an NOP command for the purposes of backward compatibility with the ANSI AT attachment standard. This command sets the Sector Count register to 0x00h.

Table 60: Wear-Level — F5h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Completion Status							
Sector Number	X							
Cylinder Low	X							
Cylinder High	X							
Drive Head	X	X	X	Drive	Flag			
Command	F5h							

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Write Multiple w/o Erase — CDh

The Write Multiple w/o Erase command functions identically to the Write Multiple command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 61: Write Multiple w/o Erase — CDh

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	CDh							

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Write Sector(s) w/o Erase — 38h

The Write Sector(s) w/o Erase command functions similar to the Write Sector command, with the exception that the implied pre-erase (i.e., Erase Sector(s) command) is not issued prior to writing the sectors.

Table 62: Write Sector(s) w/o Erase — 38h

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	38h							

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Write Verify — 3Ch

The Write Verify command verifies each sector immediately after it is written. This command performs identically to the Write Sector(s) command, with the added feature of verifying each sector written.

Table 63: Write Verify — 3Ch

Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Feature	X							
Sector Count	Sector Count							
Sector Number	Sector Number (LBA7-0)							
Cylinder Low	Cylinder Low (LBA15-8)							
Cylinder High	Cylinder High (LBA23-16)							
Drive Head	X	LBA	X	Drive	Head Number (LBA27-24)			
Command	3Ch							

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SALES AND SUPPORT

To order or obtain information on pricing and delivery, contact your SiliconSystems Sales Representative.

PART NUMBERING

NOMENCLATURE

The following table defines the SiliconDrive II 2.5" PATA Drive part numbering scheme.

Table 64: Part Numbering Nomenclature

SSD-	**D**	**YYY**	**I**	**T**	**-4300** Part number suffix — contact your SiliconSystems' Sales Representative
				Temperature Range: • Blank = Commercial • I = Industrial	
			Interface:Blank = Parallel ATA (PATA)		
		Capacity: 04G = 4GB to 32G = 32GB			
	Form Factor: D = 2.5" Drive				
SiliconSystems' **S**ilicon**D**rive					

PART NUMBERS

The following table lists the SiliconDrive II's part numbers.

Table 65: Part Numbers

Part Number	Capacity
SSD-D32G(I)-4300	32GB
SSD-D16G(I)-4300	16GB
SSD-D08G(I)-4300	8GB
SSD-D04G(I)-4300	4GB

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ROHS 6 OF 6 PRODUCT LABELING — PB-FREE IDENTIFICATION LABEL

The Pb-free identification label indicates that the enclosed components/ devices and/or assemblies do not contain any lead (i.e., they are lead-free, as defined in RoHS directive 2002/95/ED). The above symbol is on all RoHS 6 of 6 compliant product labels, as seen in Figure 16.

SAMPLE LABEL

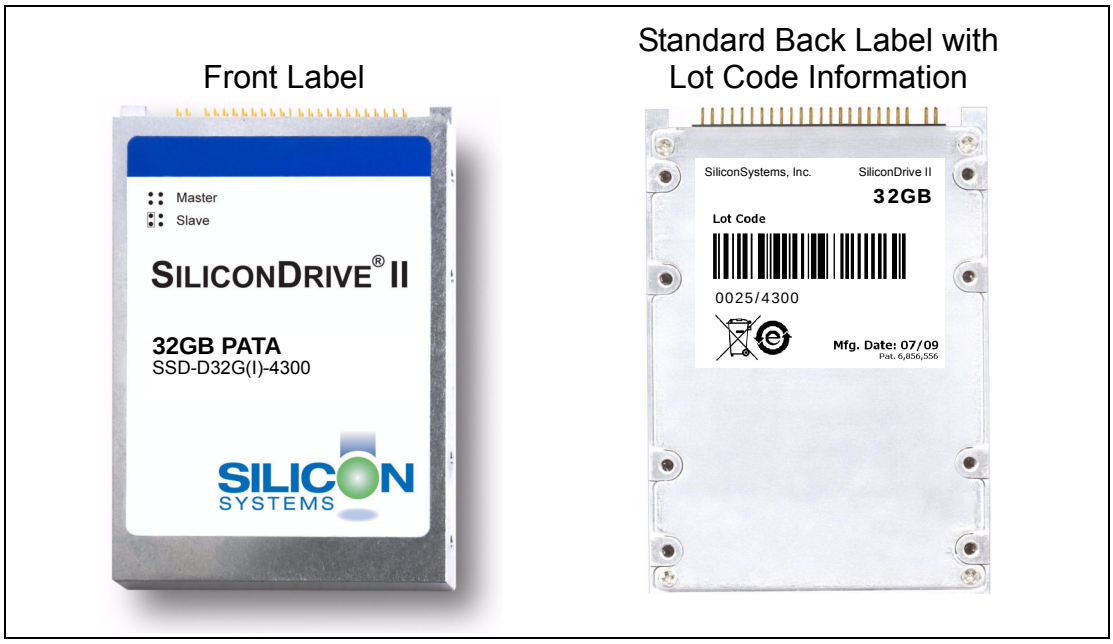

Figure 16: Sample Label

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RELATED DOCUMENTATION

For more information, visit www.siliconsystems.com or contact your SiliconSystems Sales Representative.

Table 66: Related Documentation

SiliconDrive II Application-Specific Technology	Description	Document Number
SiProtect	Protection software for password-required, read/write, or read-only access.	WP-003-0xR
SiSweep	Ultra-fast data erasure.	SiSecure-0xANR
SiPurge	Non-recoverable data erasure.	SiSecure-0xANR

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